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Thin-Film Transistor Circuits Based on Inkjet Printed Single-Walled Carbon Nanotubes and Zinc Tin Oxide

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Dedication

To my beloved parents, sisters, and wife

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Thin-Film Transistor Circuits Based on Inkjet Printed Single-Walled Carbon Nanotubes and Zinc Tin Oxide

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Recently, various novel functional materials and low-cost device fabrication techniques have emerged in the field of thin-film electronics. Active semiconductors in the form of thin-films are one of the critical components in thin-film transistors (TFTs) to achieve high-performance large-area electronics. Semiconducting single-walled carbon nanotubes (SWCNTs) and amorphous zinc tin oxide (ZTO) are considered to be some of the most promising semiconductors for TFTs due to their advantages such as high electrical performance, air-stability, and optical transparency. In this dissertation, SWCNTs and ZTO are employed as p-channel/ambipolar and n-channel semiconductors in TFTs, respectively, and integrated into various circuits through use of the cost-effective inkjet printing technique.

High-performance p-channel TFTs are demonstrated by using *single-pass* inkjet printing of SWCNTs. Dense uniform networks of SWCNTs are formed in the channel of TFTs with *single-pass* printing after application of UV O_3 treatment on the dielectric surface for suitable surface energy modification. By employing these SWCNT TFTs for p-TFTs along with ZTO n-TFTs, high-speed complementary circuits are demonstrated

with low power consumption. The material combination of high-performance inkjet printed n- and p-channel semiconductors results in the fastest ring oscillators (ROSCs) among previously reported ROSCs where printed semiconductors were utilized. Furthermore, adding additional top-gate dielectric and top-gate electrode layers on top of the ROSCs can impart new functionalities that can be used to control the oscillation frequency of the ROSCs linearly with applied top-gate bias.

Various basic circuits are also demonstrated by using inkjet printed ambipolar semiconductors. SWCNTs and ZTO, employed as p- and n-channel semiconductors for individual TFTs, turn into an ambipolar semiconductor when they are printed in a bilayer heterostructure. The bilayer ambipolar TFTs show high electron and hole mobilities in air, and ROSCs based on the ambipolar TFTs show the fastest oscillation frequency among the best reported ambipolar TFT-based ROSCs. Ambipolar SWCNT circuits are also demonstrated by encapsulating SWCNTs with aluminum oxide (Al_2O_3) layer deposited by atomic layer deposition (ALD). These ambipolar circuits are realized on flexible plastic substrates with inkjet printed electrodes, and show high operational and environmental stability.

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Chapter 1. Introduction

1.1. THIN-FILM TRANSISTORS

Thin-film transistors (TFTs) are key components in large-area electronics such as displays. In TFTs, all constituent layers, which include semiconductors, dielectrics, and electrodes, are deposited in the form of thin-films on a supporting substrate, whereas in conventional transistors the semiconductor itself is, most often, also the substrate. Because TFTs can be implemented on various substrates including plastic and paper, they are attracting great deal of attention in the field of flexible and stretchable electronics for future applications (Figure 1.1).[1-3]

A large variety of semiconducting materials including amorphous/polycrystalline silicon (Si), organic semiconductors, metal oxides, and nanowires have been widely explored as active semiconducting layers in TFTs. Among those materials, organic semiconductors have demonstrated great promises in TFTs due to their low-cost solution processability at relatively low temperature and their unlimited tunability via synthetic strategies. However, their carrier mobilities are not high enough compared to other thin-film semiconductor candidates, and conventional processing on organic semiconductors is largely limited due to their vulnerability to chemicals, moisture, and oxygen, *etc*. Generally, p-channel organic semiconductors exhibit higher performance and stability than those of n-channel organic semiconductors, although a large number of both n- and p-channel organic semiconductors have been reported.

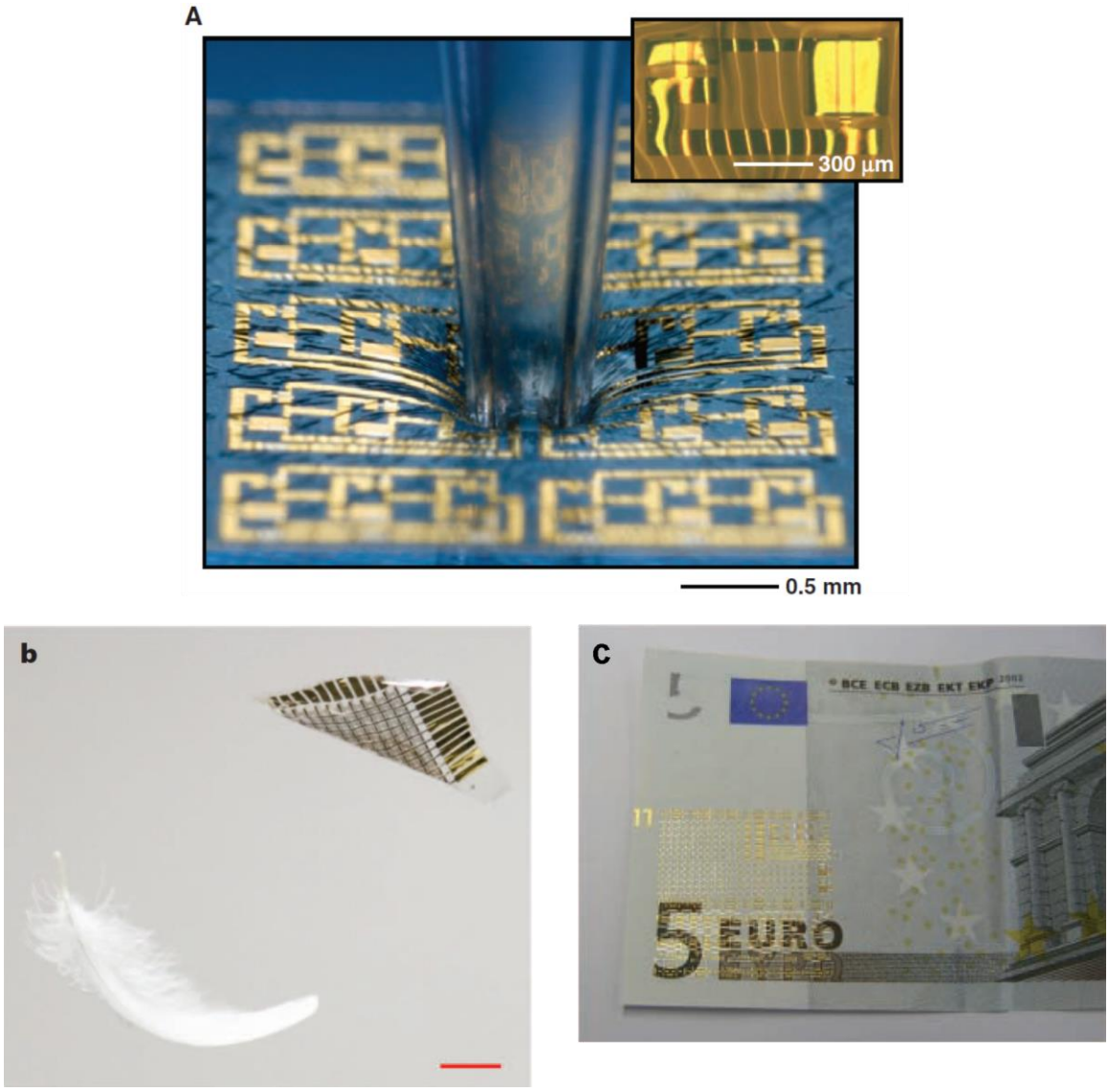

Figure 1.1: (a) Stretchable Si circuit with its compressed center (main) and wavy logic gate (top right) from ref. 1. Reprinted with permission from AAAS. (b) Ultrathin plastic electronics with extremely light weight. Reprinted with permission from Macmillan Publishers Ltd: Nature (ref. 2), copyright (2013). (c) Organic TFTs and circuits fabricated on a banknote from ref. 3. Reprinted with permission of John Wiley & Sons, Inc.

Recently, semiconducting metal oxides have emerged as high performance thin-film semiconductors. They have shown good electrical performance even in the

amorphous phase, which is preferable for large-area applications, in addition to their solution processability. Since TFTs using amorphous indium gallium zinc oxide (IGZO) were reported in 2004,[4] many different semiconducting metal oxides such as zinc tin oxide (ZTO),[5,6] and zinc indium oxide (ZIO)[7,8] have been reported. However, most of these metal oxides exhibit n-channel behavior opposite to the case of organic semiconductors.

Semiconducting single-walled carbon nanotubes (SWCNTs) are another promising candidate for thin-film semiconductors. Ballistic carrier transport, which results in extremely high carrier mobility, occurs in short channel length SWCNT devices when the channel length is much smaller than the mean free path of carriers due to their quasi-1D geometry.[9] Semiconducting SWCNTs are very promising active materials for TFTs due to their superlative electrical, mechanical, and chemical properties as well as their solution processability. For random network SWCNT TFTs ballistic transport is not applicable since the channel layer is formed by random network of SWCNTs, which have numerous tube-tube junctions. Under pristine conditions SWCNTs TFTs are ambipolar, exhibiting both p- and n-channel behavior. However, when SWCNTs are exposed to ambient air and moisture, SWCNT TFTs typically show p-channel behavior.[10-12]

Complementary metal-oxide-semiconductor (CMOS), where symmetrical and balanced pairs of n- and p-channel transistors are utilized, is the most dominant technology for constructing integrated circuits (ICs). CMOS technology has great advantages over other IC technologies such as low static power consumption, high noise immunity, and design flexibility.[13] Some circuit technologies, such as ambipolar circuits, can be designed to be complementary-like.

In this dissertation, amorphous ZTO and semiconducting SWCNTs are employed as n-channel and p-channel/ambipolar semiconductors, respectively, to construct

complementary and complementary-like circuits due to their high carrier mobilities and stabilities in air.

1.1.1. Basic thin-film transistor structure

TFTs are implemented in four basic structures as shown in Figure 1.2. The structures are categorized by the position of electrodes: gate (G) and source/drain (S/D) with respect to a semiconductor layer. In the bottom-gate structure, G is positioned under the semiconductor layer (Figure 1.2(a), (b)), while G is positioned on top of the semiconductor in the top-gate structure (Figure 1.2(c), (d)). In the bottom-contact structure, S/D contacts are formed under the semiconductor layer (Figure 1.2(a), (c)), while S/D contacts are formed on top of the semiconductor in the top-contact structure (Figure 1.2(b), (d)). The more suitable structure is carefully chosen as appropriate to the design purposes. For example, bottom-gate bottom-contact structures are usually employed in organic/polymeric TFTs when extra chemical processing on semiconductor layers is not preferable. On the other hand, TFTs in top-gate structures can show more stable operation since semiconductor layers are inherently encapsulated from outer environment.

These structures are referred to as staggered structures (Figure 1.2(b), (c)) if G and S/D are positioned at opposite sides with respect to the semiconductor layer, or coplanar structures (Figure 1.2(a), (d)) if G and S/D are positioned on the same side with respect to the semiconductor layer. In this dissertation, bottom-gate (bottom- or top-contact) structures are employed in TFTs. A double-gate structure, which has an additional dielectric layer and G electrode on top of the device, are also employed for additional gate control in Chapter 4.

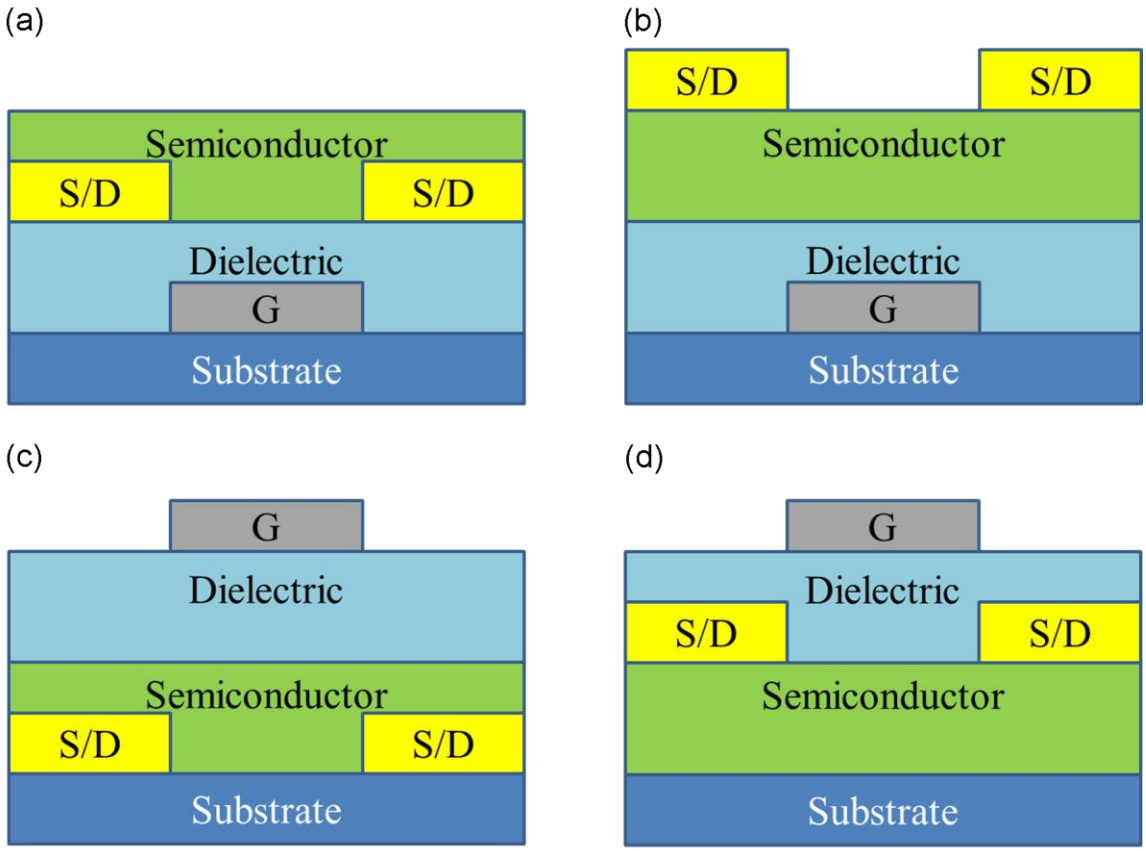

Figure 1.2: Four basic structures of TFTs. (a) Bottom-gate bottom-contact (inverted coplanar) structure. (b) Bottom-gate top-contact (inverted staggered) structure. (c) Top-gate bottom-contact (staggered) structure. (d) Top-gate top-contact (coplanar) structure.

1.1.2. Operation of thin-film transistors

TFTs operate in three regions of operation: the cutoff region, the linear region, and the saturation region. For simplicity, operation of n-TFTs will be discussed. The three regions are depicted in Figure 1.3.

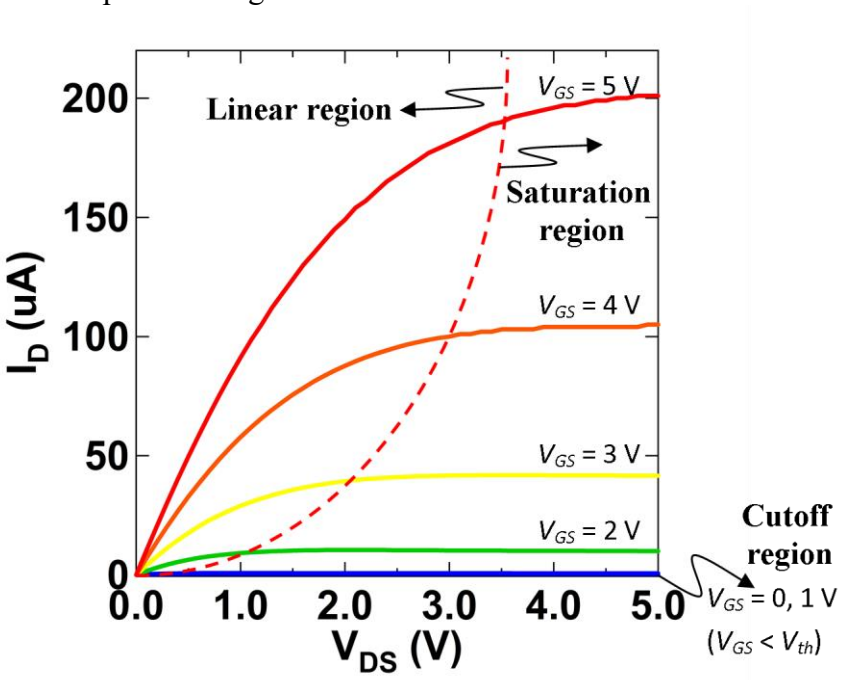

Figure 1.3: I_D-V_{DS} characteristics of an arbitrary ZTO TFT showing three regions of operation.

In the cutoff region ($V_{GS} < V_{th}$), a channel—the path for electron transport from S to D—is not formed and TFTs remain turned off. Threshold voltage (V_{th}) is the minimum required voltage to induce a channel. In real TFTs, however even below V_{th}, I_D is not completely zero as the name "cutoff region" indicates. This region before a channel is fully formed, when $V_{GS} < V_{th}$, is called the sub-threshold region. The sharp increase of I_D with V_{GS} is related to the density of trap states in the semiconductor and is called sub-threshold swing. In the case of disordered semiconductor based TFTs, the sub-threshold

region can be further divided by type of carrier transport into a diffusion-limited region and a drift-limited region as shown in Figure 1.4.

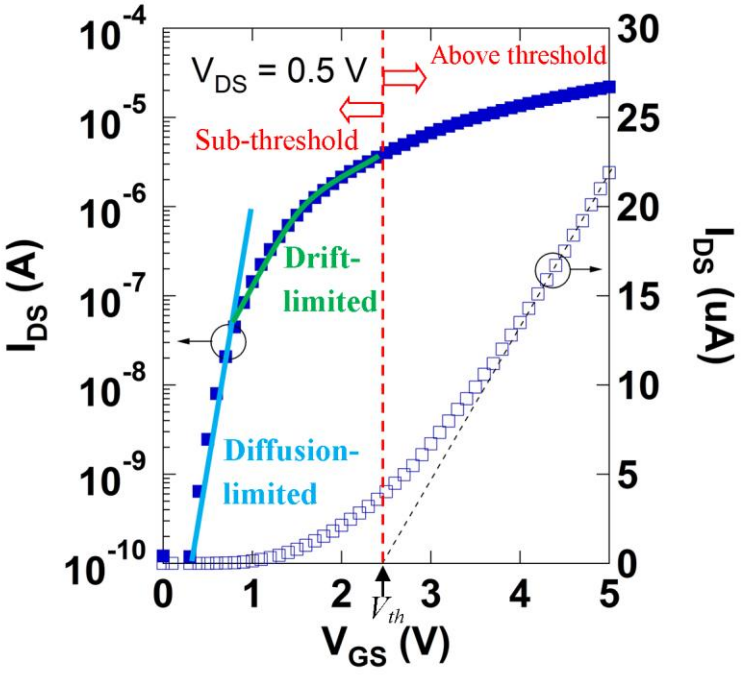

Figure 1.4: I_D-V_{GS} characteristics of an arbitrary ZTO TFT showing three regions of operation: (i) Diffusion-limited sub-threshold region. (ii) Drift-limited sub-threshold region. (iii) Above threshold region. Intercept of the black dotted line indicates a threshold voltage of the TFT.

When $V_{GS} = V_{th}$, electrons accumulate at the interface between dielectric and semiconductor layers and form a channel as shown in Figure 1.5(a). If a voltage difference is set between S and D, electrons start to move in the channel from S to D and current flows from D to S. When small V_{DS} is applied, the channel conductance increases proportional to $V_{GS} - V_{th}$. This region of operation is called the linear region (Figure 1.3) or the above threshold region (Figure 1.4). In the linear region (when $V_{GS} \geq V_{th}$ and $V_{DS} < V_{GS} - V_{th}$), drain current I_D is expressed by the following basic equation (eq 1.1):

$$I_D = \mu C_{ox} \frac{W}{L} \{(V_{GS} - V_{th})V_{DS} - \frac{1}{2} V_{DS}^{\ 2}\} \qquad \text{(eq 1.1)}$$

where μ is the mobility of carriers, C_{ox} is the capacitance of the dielectric per unit area, W is the channel width, and L is the channel length.

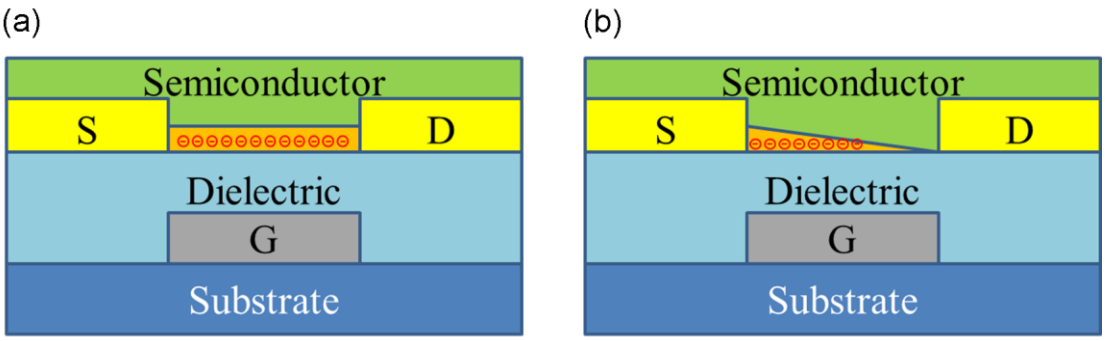

Figure 1.5: Schematic cross-section of a n-TFT (a) in the linear region (the channel, in orange, is induced) and (b) in the saturation region (the channel is pinched off from drain end).

Induced channel profile starts becoming non-uniform at D end when V_{DS} increases with fixed V_{GS} since voltage difference between G and D decreases. When $V_{GS} - V_{DS} = V_{th}$, the channel is pinched off as shown in Figure 1.5(b). After the pinch-off occurs in the channel, the channel resistance becomes almost infinite and I_D becomes almost independent of V_{DS}. This region of operation is called the saturation region. In the saturation region (when $V_{GS} \geq V_{th}$ and $V_{DS} \geq V_{GS} - V_{th}$), drain current I_D is expressed by the following equation (eq 1.2):

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 \qquad \text{(eq 1.2)}$$

Field-effect mobilities μ can be extracted by using $\partial I_D / \partial V_{GS}$ and $\sqrt{I_D}$ -V_{GS} characteristics in the linear and saturation regions, respectively, from the experimental data.

1.2. CARBON NANOTUBES

Carbon Nanotubes (CNTs) are allotropes of carbon with a quasi-1D cylindrical structure. Their very small diameter (ranging from 0.5 to 5 nm) with high aspect ratio allows carriers to be confined only along length axis. CNTs are categorized by two families: single-walled and multi-walled CNTs (SWCNTs and MWCNTs). In this dissertation, SWCNTs are the main concern since semiconducting SWCNTs are employed as active layers in electronic applications, whereas MWCNTs are usually zero-gap metals.

The chirality of SWCNTs is described by a pair of indices (n, m), where n and m are the number of unit vectors in the lattice of graphene to define the chiral vector $\mathbf{C_h}$ as shown in Figure 1.6. Any two lattice points of a graphene sheet, which $\mathbf{C_h}$ connects, are coincidental when the graphene sheet is "rolled-up" into the CNT. $\mathbf{C_h}$ is expressed by the equation (eq 1.3):[9]

$$\mathbf{C_h} = n\mathbf{a_1} + m\mathbf{a_2} = (n, m), (n, m \text{ are positive integers}, 0 \leq m \leq n) \qquad \text{(eq 1.3)}$$

where $\mathbf{a_1}$ and $\mathbf{a_2}$ are the primitive lattice vectors of graphene. The translational vector $\mathbf{T}$, which denotes the SWCNT axis, is defined as the smallest graphene lattice vector perpendicular to $\mathbf{C_h}$. Figure 1.6 shows an example of a (4, 2) SWCNT construction, and its $\mathbf{C_h}$ and $\mathbf{T}$.

In general, if $n - m$ is an integer multiple of 3, the SWCNTs exhibit metallic properties. Therefore, about one-third of as-synthesized SWCNTs are metallic, and only the other two-third are semiconducting. Use of as-synthesized SWCNTs, without sorting out metallic species, as an active channel material in TFTs results in poor I_{on}/I_{off} and device failure by forming conduction paths of current on which gate modulation has no effect. Many approaches have been proposed to effectively sort semiconducting nanotube species from metallic.[14-18]

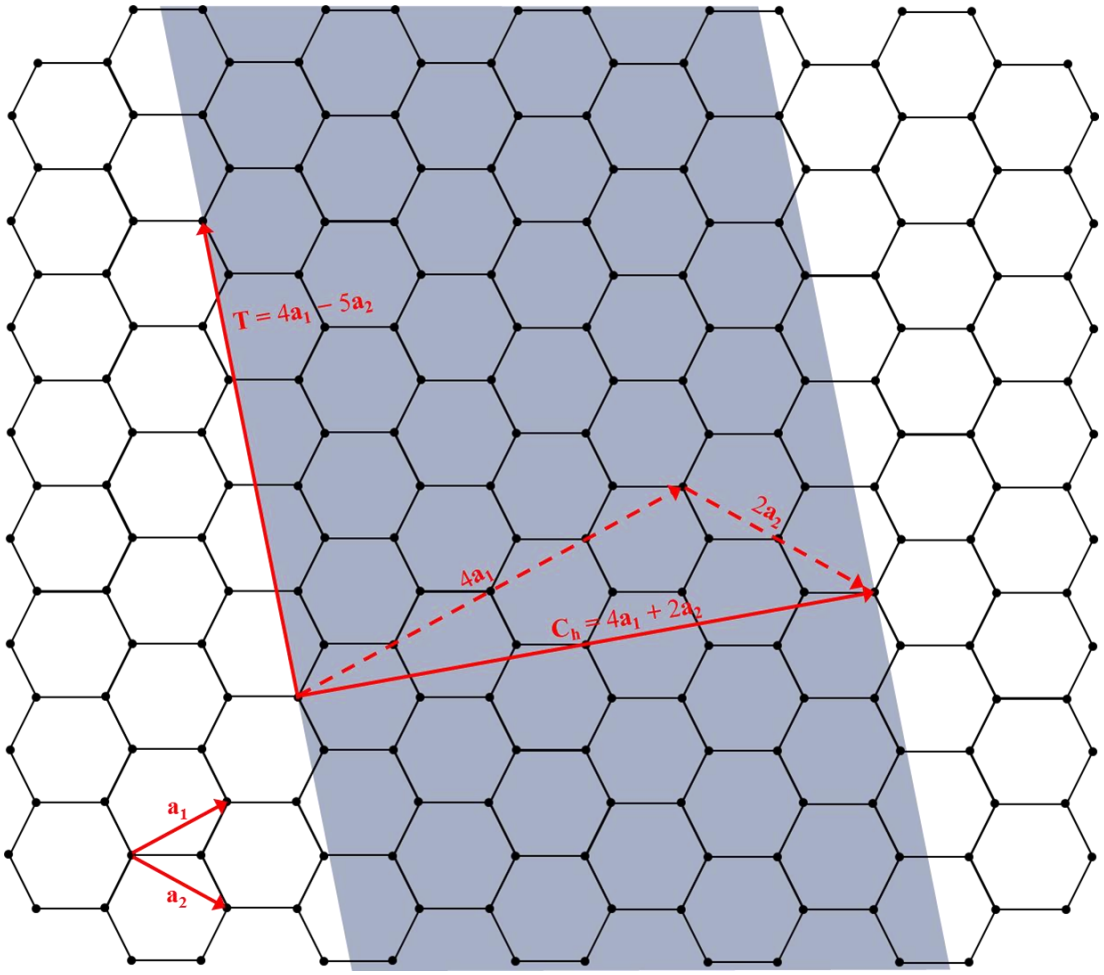

Figure 1.6: Conceptual illustration of a (4, 2) SWCNT construction. If shaded area of a graphene sheet is "rolled-up" to make the start and end points of C_h are coincided, the (4, 2) SWCNT is created.

In 2006, Hersam *et al*. successfully demonstrated a scalable semiconducting SWCNT sorting technique by using density-gradient ultracentrifugation (DGU).[15] By dispersing SWCNTs in solutions of surfactants such as sodium cholate and sodium dodecyl sulphate, the surfactants interact with the SWCNT surface and the SWCNTs are encapsulated by the surfactants as shown in Figure 1.7(a). Upon ultracentrifugation of the encapsulated SWCNTs, they are separated into multiple regions with bands of various

colors by differences in their buoyant densities as shown in Figure 1.7(b). High purity semiconducting SWCNTs >97% have been harvested within very narrow diameter range by using this technique. A chirality-based separation method has been further developed based on this technique.[16]

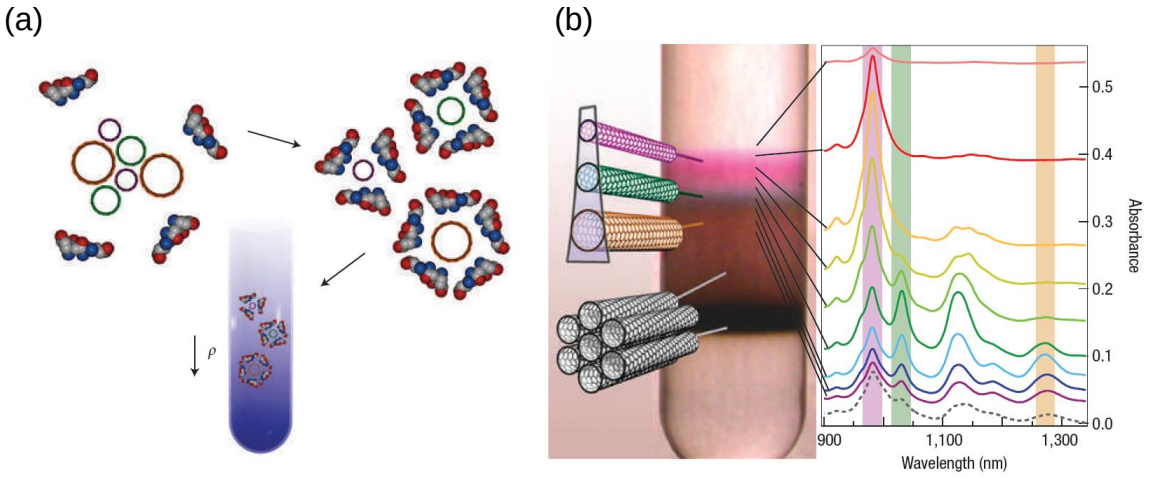

Figure 1.7: (a) Schematic of surfactant encapsulation and sorting by created density gradient. (b) Sorted SWCNTs in various colored bands and their optical absorbance spectra. Reprinted with permission from Macmillan Publishers Ltd: Nature Nanotechnology (ref. 15), copyright (2006).

SWCNTs used in this dissertation were sorted by using DGU with semiconducting purity >98% and provided by Dr. Hersam's group at Northwestern University. A small fraction of metallic SWCNTs still exists in the channel of TFTs, but it does not severely affect I_{off} since the channel lengths of random network TFTs in this dissertation are much longer than the lengths of SWCNTs. Sorted SWCNTs can be dispersed in various solutions such as aqueous solutions[19,20] and organic solvents,[21,22] and deposited by cost-effective solution process. In this dissertation, SWCNTs are dispersed in 1-cyclohexyl-2-pyrrolidone (CHP) and deposited by inkjet printing to make p-channel or ambipolar TFTs.

1.3. METAL OXIDE SEMICONDUCTORS

The concept of designing transparent amorphous semiconducting metal oxides was firstly proposed by Hosono *et al.* in 1996.[23,24] Semiconductors in the amorphous phase are preferable to crystalline semiconductors in large-area electronics due to advantages such as uniformity in device characteristics, low-cost, and low-temperature processability. However, amorphous materials with high conductivity in addition to high transparency were difficult to find since their carrier mobilities were several orders lower than crystalline materials'.

In 2004, Hosono *et al.* successfully demonstrated high performance transparent TFTs using amorphous IGZO at room temperature.[4] In this amorphous metal oxide semiconductor, electron transport paths (conduction band minima) are composed of spherical post-transition-metal *s* orbitals as shown in Figure 1.8(b). Large overlap between neighboring metal *ns* (where *n* is the principal quantum number) orbitals allow highly efficient electron transport even with distorted chemical bonds in amorphous phases. The magnitude of overlap is insensitive to its crystallinity, therefore, carrier mobility of amorphous IGZO is similar to that of crystalline IGZO. In contrast, electron transport paths in covalent semiconductors such as Si are composed of highly directive sp^3 hybrid orbitals as shown in 1.8(a). Distortions in its chemical bonds significantly reduce the magnitude of bond overlaps and the carrier mobility in covalent amorphous semiconductors is greatly degraded compared to the mobility in covalent crystalline semiconductors.

Most of metal oxide semiconductors exhibit n-channel behavior, although a p-channel oxide semiconductor, SnO, has been reported.[25,26] This is because hole transport paths (valence band maxima) are mainly composed of localized oxygen 2*p* orbitals, whereas electron transport paths are predominantly composed of spatially spread metal *ns*

orbitals in metal oxide semiconductors. Therefore, it is more challenging to achieve high performance in p-channel metal oxide semiconductors as high as in n-channel metal oxide semiconductors.

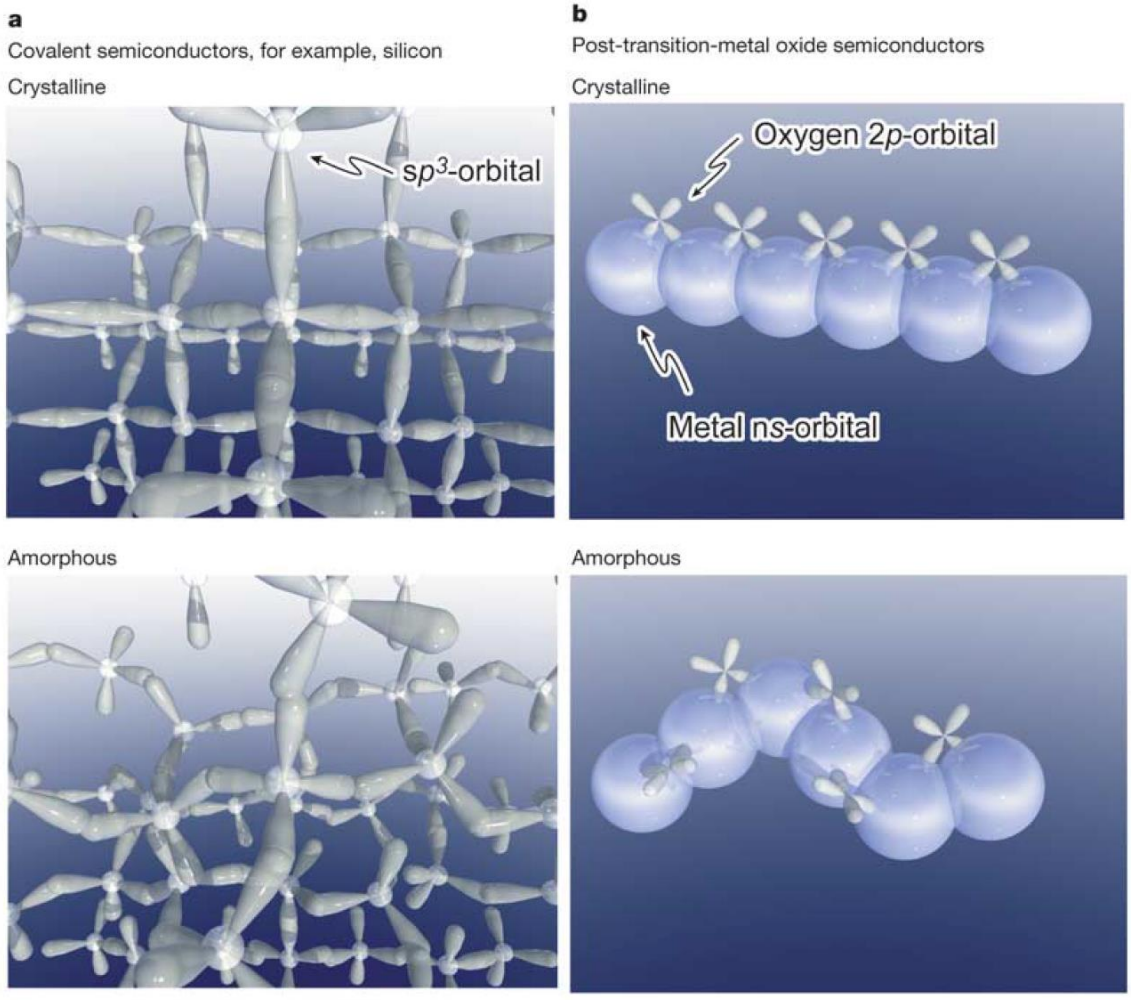

Figure 1.8: Schematic of orbitals for carrier transport in (a) covalent semiconductors and (b) metal oxide semiconductors. Reprinted with permission from Macmillan Publishers Ltd: Nature (ref. 4), copyright (2004).

Metal oxide semiconductors can be also deposited by simple and cost-effective solution processes such as spin-coating and inkjet printing.[27-30] In this dissertation,

amorphous ZTO are employed as a n-channel semiconductor and deposited by inkjet printing.

1.4. OUTLINE OF DISSERTATION

This dissertation describes various thin-film TFT-based circuits created using inkjet printed semiconductors. The dissertation is composed of seven chapters.

Chapter 2 describes high-performance SWCNT TFTs—one of basic elements in the circuits presented in later chapters—fabricated by *single-pass* inkjet printing on the solution-processed ZrO_2 gate dielectric. It is shown that UV O_3 treatment on the dielectric layer is critical for achieving a uniform dispersion of sorted SWCNTs in the semiconducting channel. High-performance characteristics of SWCNT TFTs are reproduced in a large number of TFTs.

Chapter 3 demonstrates that the materials combination of inkjet printed SWCNTs and ZTO is very promising for large-area thin-film electronics by implementing high-speed complementary circuits. The signal delay per stage of 140 ns for complementary ring oscillators (ROSCs) is the fastest reported for any ROSC circuit with printed semiconductors to date.

Chapter 4 describes voltage-controlled ROSCs with double-gate complementary transistors where both the n- and p-channel semiconductors are deposited by inkjet printing. Top gates added to conventional ROSC circuits control not only threshold voltages of the constituent transistors but also the oscillation frequencies of the ROSCs. The oscillation frequency increases or decreases linearly with applied top gate potential.

Chapter 5 illustrates ambipolar field-effect transistors (FETs) consisting of inkjet printed semiconductor bilayer heterostructures by utilizing SWCNTs and ZTO. Electron

transports occur principally in the oxide layer and hole transports occur exclusively in the SWCNT layer. ROSCs comprised of bilayer ambipolar transistors demonstrate the fastest oscillation frequency among previously reported ambipolar ROSCs.

Chapter 6 describes inkjet printed ambipolar SWCNT TFTs and circuits with high operational stability on flexible and rigid substrates. All patterns—electrodes, semiconductors, vias—are realized by inkjet printing without the use of rigid physical masks and photolithography. An Al_2O_3 layer deposited on devices by atomic layer deposition (ALD) transforms p-type SWCNT TFTs into ambipolar SWCNT TFTs and encapsulates them effectively.

Finally, Chapter 7 summarizes the conclusions drawn from this study.

Chapter 2. Thin-Film Transistors Based on Inkjet Printed Carbon Nanotubes*

2.1. INTRODUCTION

Inkjet printing based fabrication technology has been attracting great interest for use in various applications such as thin-film transistors (TFTs), light emitting diodes, solar cells, and sensors.[31-35] The advantages of this technology include additive patterning, reduction of material waste, and compatibility with flexible and large area substrates. This printing technology can lead to a substantial reduction in cost and time in electronics manufacturing because patterns can be directly drawn on targeted locations without a pre-patterning process and can be easily altered. Recently, novel active materials, such as conjugated polymers[31-34] and semiconducting metal oxides,[27,30] have been explored for inkjet printing applications.

Single-walled carbon nanotube (SWCNT) TFTs are expected to enable the next generation high-performance, flexible electronic devices due to their superlative properties, such as high chemical stability, high carrier mobility, transparency, and remarkable mechanical properties.[18] However, as-synthesized SWCNTs usually contain both metallic and semiconducting species leading to a compromise between charge-carrier mobility and ON/OFF current ratio (I_{on}/I_{off}). In recent years, several approaches have been demonstrated which effectively separate metallic and semiconducting

*This chapter is based on Reference 22: Kim, B.; Jang, S.; Prabhumirashi, P. L.; Geier, M. L.; Hersam, M. C.; Dodabalapur, A. Low Voltage, High Performance Inkjet Printed Carbon Nanotube Transistors with Solution Processed ZrO_2 Gate Insulator. *Appl. Phys. Lett.* **2013**, *103*, 082119. B.K., S.J., and A.D. designed the experiments. B.K. carried out fabrication and characterization of devices. S.J. took data on surface energies and helped with SWCNT inkjet printing. P.L.P., M.L.G., and M.C.H. provided semiconducting SWCNTs, and took SEM images and optical absorbance spectra data of SWCNTs.

SWCNTs.[15-18] These separation schemes result in predominantly semiconducting SWCNT films that enable TFTs with low OFF currents due to reduction in metallic percolating pathways and improved gate modulation. When integrated with high-κ dielectrics, these TFTs can achieve high mobilities, improved transconductance, and high I_{on}/I_{off} at low operating voltages.[36]

For successful inkjet printing of SWCNTs, it is critical that the ink wets the targeted surface uniformly since networks of SWCNTs are formed during the drying of the ink. To deposit high density and uniform SWCNT films on SiO_2, approaches such as surface functionalization with (3-aminopropyl) triethoxysilane[37,38] and poly-L-lysine[39,40] have been proposed. To avoid SWCNT bundling, sequential inkjet printing multiple times (> 15 times) with a very low concentration ink has also been attempted. Using these strategies, several research groups have reported inkjet printed SWCNT TFTs;[21,41-46] however, the electrical performance of the resulting devices has been relatively poor compared to other solution based deposition methods.[19,20,47] Recently, one research group has demonstrated high-performance SWCNT TFTs via multiple inkjet printing (>100 times) on a conventional vacuum-deposited HfO_2 dielectric.[44] However, this approach has limited scalability since rinsing and drying steps are needed after each printing cycle.

Herein, we report fabrication of high-performance SWCNT TFTs via *single-pass* inkjet printing on solution-processed ZrO_2 high-κ dielectrics. This significant advance is enabled by an ultraviolet (UV) O_3 treatment that tailors the surface properties of ZrO_2 for uniform SWCNT coverage. These TFTs exhibit high intrinsic mobilities, exceeding 30 $cm^2 V^{-1} s^{-1}$, and an $I_{on}/I_{off} > 10^4$ at low operating voltages (< 5 V). Notably, this mobility value exceeds all previous reports for *single-pass* inkjet printing not only for SWCNT TFTs but also other TFT technologies including polymers[31,32] and metal oxides.[27,30]

2.2. EXPERIMENTAL

2.2.1. Preparation of SWCNT inks

High-purity semiconducting SWCNT inks dispersed in aqueous media were synthesized by dual-iteration DGU[15,16] using electric arc-discharge grown (P2, Carbon Solutions Inc.) SWCNTs. After ultracentrifugation, the centrifuge tubes were fractionated in 0.5 mm steps using a piston gradient fractionator (Biocomp Instruments Inc.), and the SWCNT electronic type purity of individual fractions was determined by optical absorbance spectroscopy (Varian Cary 5000 spectrophotometer). The fractions corresponding to semiconducting purity of >98% were combined to make the resulting SWCNT ink solution. The SWCNT ink was then dialyzed (Slide-A-Lyzer Dialysis Cassettes, 20K MWCO, 0.5mL, Pierce Biotechnology, Inc.) into 1% w v^{-1} sodium cholate aqueous solution in order to remove the density gradient medium (iodixanol). After dialysis, the high-purity semiconducting ink was subsequently used to fabricate a SWCNT buckypaper via vacuum filtration through a porous nylon membrane (Whatman WNYL, 0.2 μm), followed by copious rinsing with nanopure water (18.2 MΩ-cm resistivity) to remove surfactants from the SWCNTs. Once dry, the SWCNT buckypaper was first dispersed in 1-cyclohexyl-2-pyrrolidone (CHP) and then ultrasonicated in a bath-type ultrasonic cleaner for 6 h to make a uniform suspension. The concentration of SWCNTs in the ink was 0.1 mg mL^{-1}. Before inkjet printing, the ink was ultrasonicated again for more than 2 h to form a uniform dispersion of SWCNTs in CHP.

2.2.2. Deposition of ZrO_2

Zirconium chloride ($ZrCl_4$) and zirconium isopropoxide iso-propanol complex [$Zr(OCH(CH_3)_2)_4 \cdot (CH_3)_2CHOH$] powders were dissolved in 2-methoxyethanol to prepare the ZrO_2 precursor solution.[48] These metal precursors had a molar ratio of 1.0 in

a solution with concentration of 0.5 M. The solution was stirred to obtain uniformly dissolved solution for 24 h before deposition. The prepared solution was deposited on a Si substrate by spin coating at a spin speed of 2000 rpm for 1 min in N_2 environment. Following this step, the substrate was annealed on a hotplate at 500 °C for 1 h in air. The same procedure was repeated to obtain a double layer of ZrO_2 film.

2.2.3. TFT fabrication

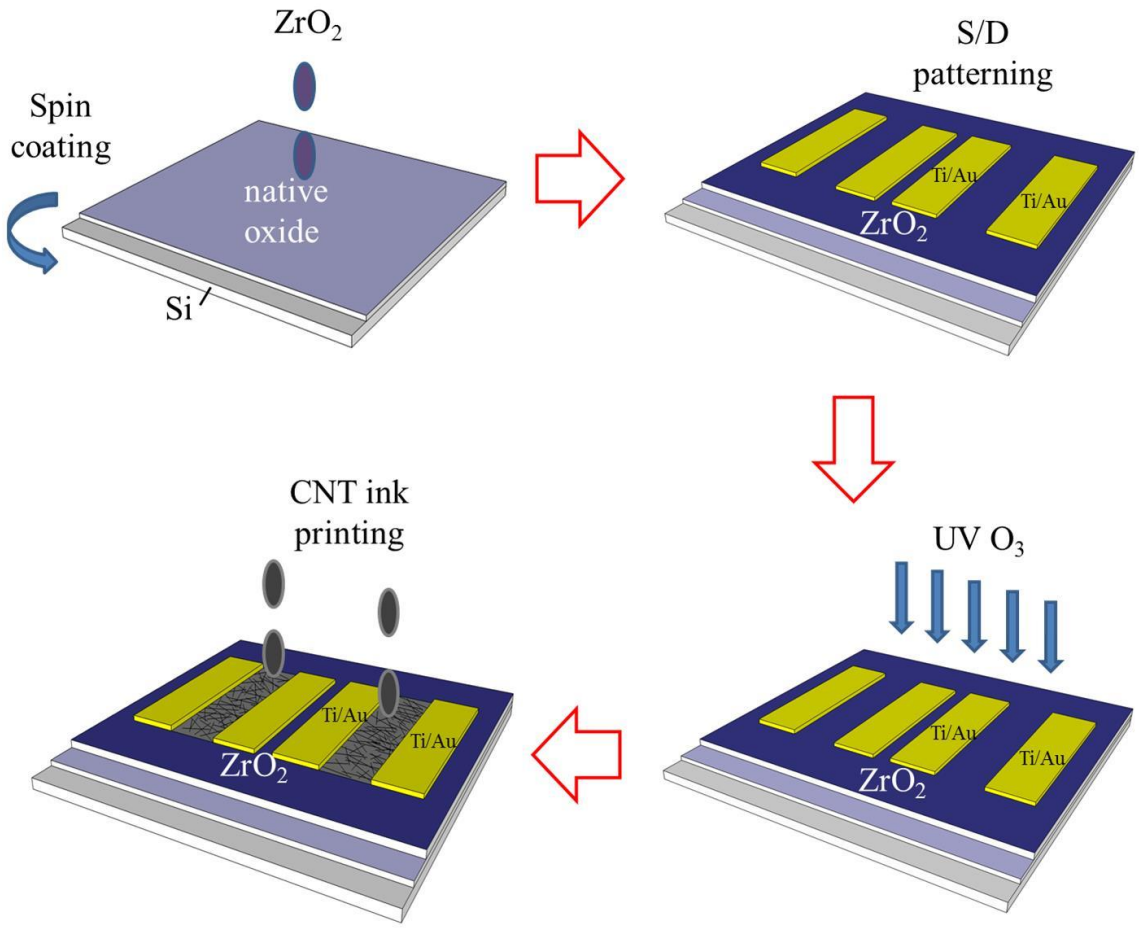

Figure 2.1: The process of inkjet printed SWCNT TFT fabrication.

The SWCNT TFT fabrication process is illustrated in Figure 2.1. ZrO_2 was deposited by sequential spin coating on a Si substrate. The TFT S/D electrodes were

defined by photolithography and a Ti/Au (3 nm/30 nm) bilayer was deposited sequentially by thermal evaporation. Following this step, the dielectric film was UV O_3 treated for 10 min using a bench top UV cleaner (Novascan PSD-UVT). The SWCNT ink was inkjet printed using a FUJIFILM Dimatix 2800 printer at room temperature in air. The volume of each droplet was 10 pL, and the drop spacing was chosen to be 40 μm. The diameter of each drop was 60–70 μm as printed. After printing, the ink was dried on a hotplate at 200 °C for 30 min in air to remove residual solvents.

2.3. RESULTS AND DISCUSSION

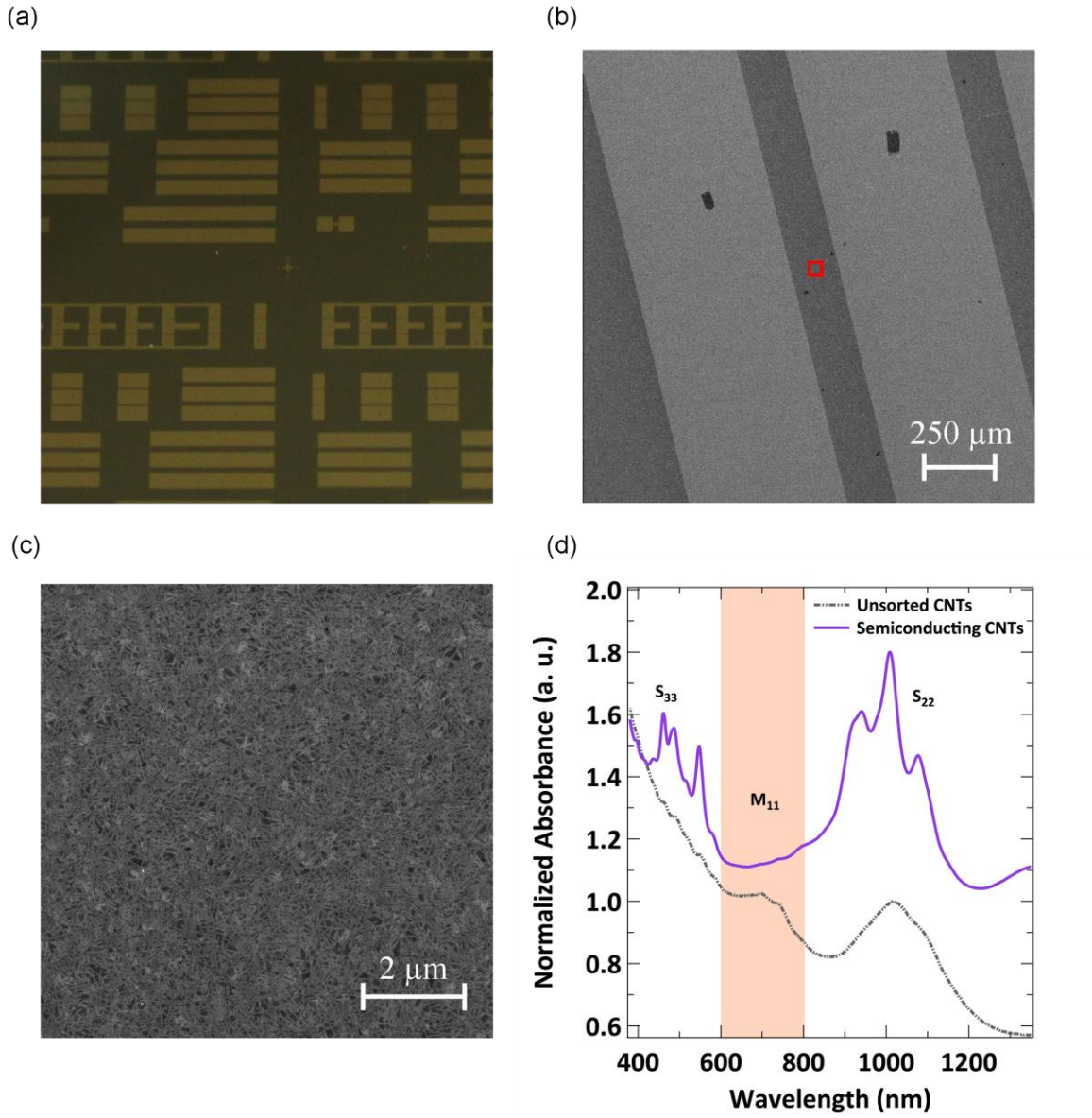

Figure 2.2: (a) Optical image of the SWCNT TFT array. (b) Low-magnification SEM image of a SWCNT TFT (L=150 µm, W=3000 µm). (c) SEM image of SWCNT distribution in the channel area (red square in (b)). (d) Optical absorbance spectra of the SWCNT ink.

Figure 2.2(a) shows an optical image of the SWCNT TFT array. The array has several TFTs possessing different channel lengths, *L (varying from 20 µm to 250 µm),*

and channel width, *W (W/L = 20)*. Figure 2.2(b) shows the low-magnification scanning electron micrograph of a SWCNT TFT with *L* of 150 μm and *W* of 3000 μm. Figure 2.2(c) is a higher magnification scanning electron micrograph displaying dense and uniform networks of SWCNTs in the channel. Figure 2.2(d) shows the optical absorbance spectra for sorted semiconducting and unsorted SWCNTs respectively. The purity of the SWCNTs is determined to be >98% by comparing the areas under the metallic (M_{11}) and semiconducting (S_{22}) optical transitions.

Uniformly distributed networks of SWCNTs are essential to obtain high-performance TFTs. Sparse networks of SWCNTs cannot transport carriers effectively and thick SWCNT bundles can cause high OFF currents due to poor gate control as a consequence of tube to tube screening. In our SWCNT TFT structures, UV O_3 treatment was applied to the ZrO_2 surface to promote the wetting of the SWCNT ink by rendering the surface hydrophilic.[49] To observe the effect of UV O_3 treatment on solution processed ZrO_2, the contact angle formed by H_2O and ethylene glycol drops on ZrO_2 was measured before and after the treatment. The surface energy, calculated using measured contact angles, increased by ~60% (from 48.3 mJ m^{-2} to 75.9 mJ m^{-2}) after the UV O_3 treatment. This indicates that the UV O_3 treatment changed the conditions of the ZrO_2 surface to make it hydrophilic, which helps the SWCNT ink wet the surface uniformly. The effect of UV O_3 treatment on the wetting of the SWCNT ink on ZrO_2 is shown in Figure 2.3. A straight line pattern of SWCNT ink was inkjet printed on ZrO_2, which has both untreated and UV O_3 treated regions. The SWCNT ink on untreated ZrO_2 was separated into several large droplets after printing (Right), while the SWCNT ink on UV O_3 treated ZrO_2 remains in a continuous line (Left).

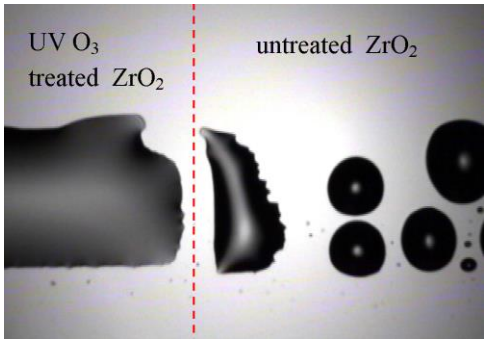

Figure 2.3: Optical image of the printed SWCNT ink on untreated and UV O_3 treated ZrO_2.

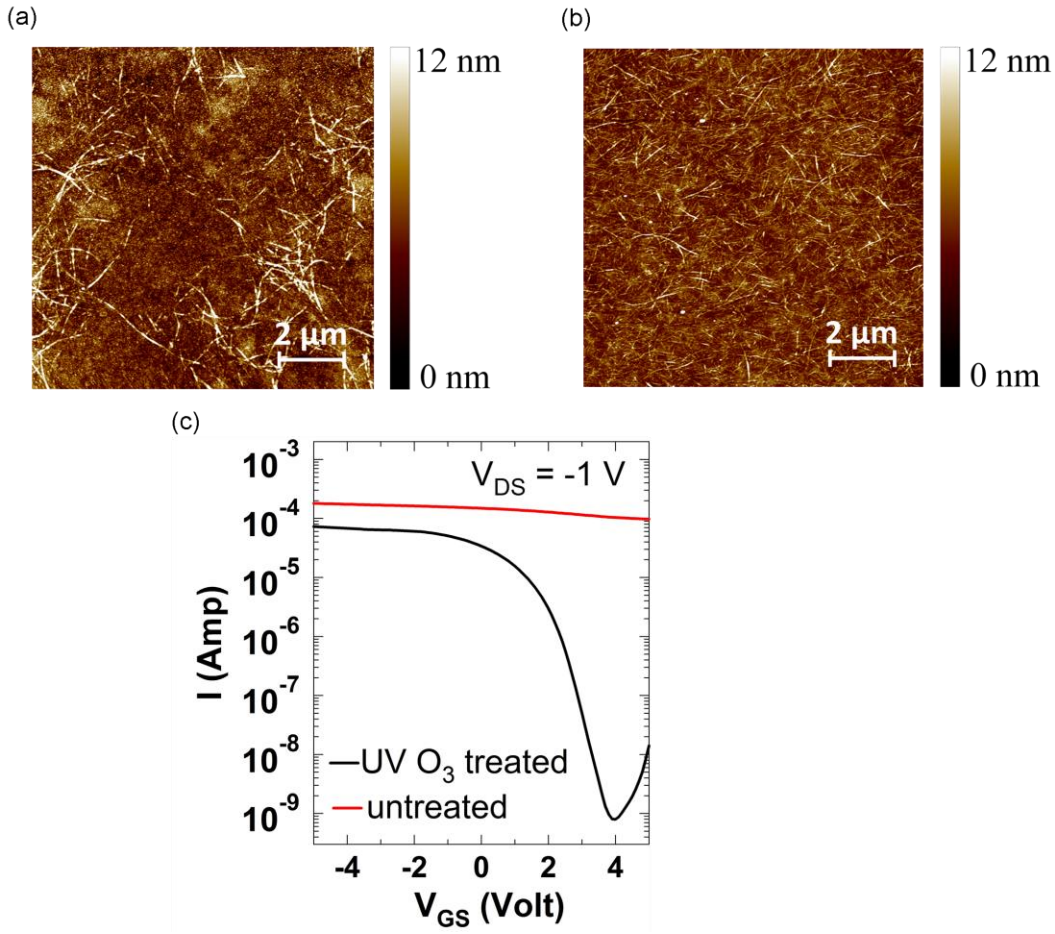

Figure 2.4: (a) AFM image of the SWCNT network on untreated ZrO_2. (b) AFM image of the SWCNT network on UV O_3 treated ZrO_2. (c) Transfer characteristics of untreated and UV O_3 treated SWCNT TFTs.

Figure 2.4(a) and (b) show the atomic force microscopy (AFM) images of the inkjet printed SWCNT network on untreated and UV O_3 treated ZrO_2, respectively. It can be clearly observed that significant areas remain uncovered (with SWCNTs) on pristine ZrO_2, Figure 2.4(a). After the UV O_3 treatment, inkjet printed SWCNT film coverage is uniform and densely distributed as shown in Figure 2.4(b). Figure 2.4(c) displays the substantial difference in transfer characteristics between UV O_3 treated and untreated devices. The gate modulation of the channel current in the UV O_3 treated devices is strong, with an I_{on}/I_{off} of 9.1×10^4, whereas in the untreated device there is very little gate modulation of the drain current. This gate-voltage-independent high current in the untreated devices may be due to the aggregation of SWCNTs in thick bundles resulting in very poor gate control due to screening.

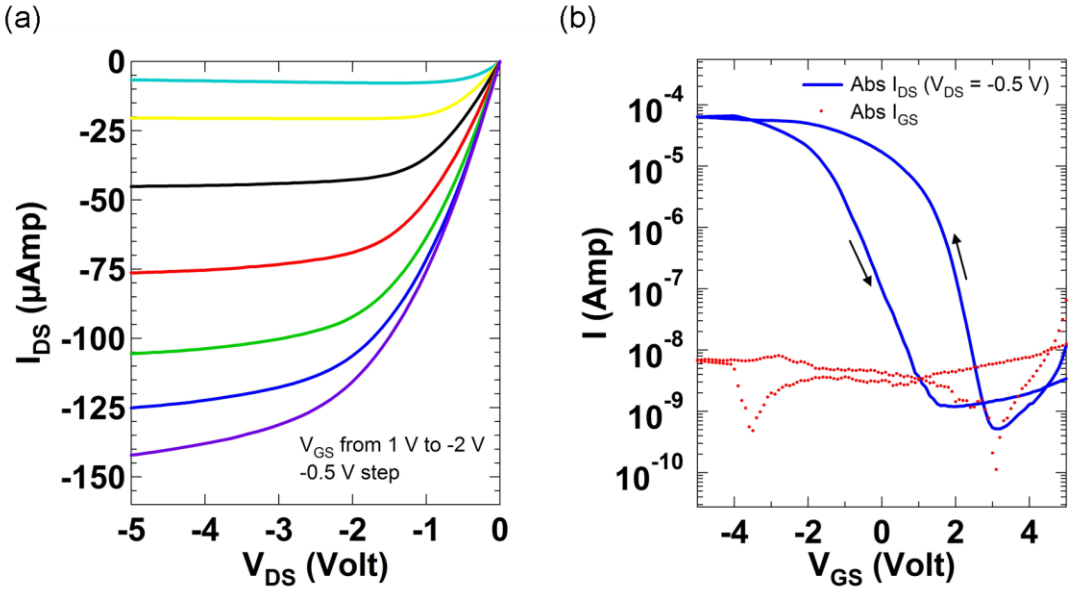

Figure 2.5: (a) Output characteristics of the inkjet printed SWCNT TFT (L=150 μm, W=3000 μm). (b) Transfer characteristics of the inkjet printed SWCNT TFT (L=150 μm, W=3000 μm). I_{on}/I_{off} is larger than 10^5 for this device.

The TFT measurements were performed in ambient conditions using a HP 4155C semiconductor parameter analyzer. Figure 2.5(a) and (b) show typical output and transfer characteristics of a SWCNT TFT with L = 150 μm and W = 3000 μm. The operating voltage is low due to the high-κ dielectric ZrO_2 with clearly observed linear and saturation regions. The shape of the output curve at low drain voltages (V_D < −0.5 V) is linear, indicating that the contact resistance between SWCNTs and the S/D electrodes is negligible. The transfer characteristic (Figure 2.5(b)) was measured between gate voltages of 5 V and −5 V with a fixed drain bias of −0.5 V. This device exhibits a high intrinsic mobility of 23.6 $cm^2 V^{-1} s^{-1}$, I_{on}/I_{off} of 1.2×10^5, and a threshold voltage of 3.1 V. In other samples with a top contact geometry, the mobility was as high as 38.6 $cm^2 V^{-1} s^{-1}$. The mobility value in these devices was extracted from the characteristics shown in Figure 2.5(b) by the following equation:

$$\mu = \frac{L}{W} \times \frac{1}{C_{net-ox}} \times \frac{1}{V_D} \times \frac{dI_D}{dV_G} \qquad \text{(eq 2.1)}$$

where μ is linear field-effect mobility, $C_{net\text{-}ox}$ is the total capacitance per unit area, V_D is the drain voltage, I_D is the drain current and V_G is the gate voltage. Since there is a thin native oxide layer covering the Si, the net effective capacitance of ZrO_2/native oxide, $C_{net\text{-}ox}$, was obtained from equation (eq 2.2):

$$\frac{1}{C_{net-ox}} = \frac{1}{C_{native-ox}} + \frac{1}{C_{ZrO_2}} \qquad \text{(eq 2.2)}$$

The capacitance of each dielectric per unit area C_i is extracted by a parallel plate capacitance model, $C_i = \varepsilon_0 \kappa_i / t_i$ with ε_0 is the vacuum permittivity, κ_i is dielectric constant of each dielectric layer, and t_i is the thickness of each dielectric layer. The thickness of the native oxide and ZrO_2 were measured to be 4.6 nm and 90 (± 4) nm by ellipsometry and depth profiles on calibration samples, respectively. The dielectric constant of SiO_2 is known to be 3.9 and the dielectric constant of solution processed ZrO_2 was calculated to

be 22.4. $C_{net\text{-}ox}$, $t_{net\text{-}ox}$ and $\kappa_{net\text{-}ox}$ were determined to be 170 nF cm^{-2}, 94.6 nm and 18.2, respectively. The field effect mobility, calculated using the parallel plate capacitance model, is 10.5 cm^2 V^{-1} s^{-1}.

For SWCNT transistors, a more rigorous capacitance model is required to obtain the intrinsic capacitance of SWCNT films due to their limited surface coverage and cylindrical geometry. The parallel plate capacitance model typically underestimates the mobility due to an overestimation of capacitance. The degree of the overestimation is more severe in the case of high-κ dielectrics and sparse SWCNT networks.[36] The intrinsic capacitance is defined in equation (eq 2.3) by considering the effect of electrostatic coupling between SWCNTs:

$$C_{net-ox} = \{\frac{1}{2\pi\varepsilon_0\varepsilon_{net-ox}} \times \ln[\frac{\Lambda_0}{R} \times \frac{\sinh(\frac{2\pi t_{net-ox}}{\Lambda_0})}{\pi}] + C_Q^{-1}\}^{-1} \times \Lambda_0^{-1} \qquad \text{(eq 2.3)}$$

where Λ_0^{-1} is the linear density of CNTs, $C_Q = 4.0\times10^{-10}$ F m^{-1} is the quantum capacitance of SWCNTs[50,51] and $R = 0.72$ nm is the average radius of SWCNTs. Λ_0^{-1} was measured to be around 8 tubes/μm from four different AFM images of SWCNT network. Five equally spaced lines are drawn on the AFM image in both the vertical and horizontal directions. The number of SWCNTs which intersect the line are counted and divided by the length of the line. An intrinsic capacitance value of 76 nF cm^{-2} was obtained by equation (eq 2.3). The intrinsic $C_{net\text{-}ox}$ was found to be approximately 45% of $C_{net\text{-}ox}$ in the parallel plate model. Consequently, an intrinsic mobility of 23.6 cm^2 V^{-1} s^{-1} was calculated. This high mobility reflects the dense and uniform SWCNT network in the channel.

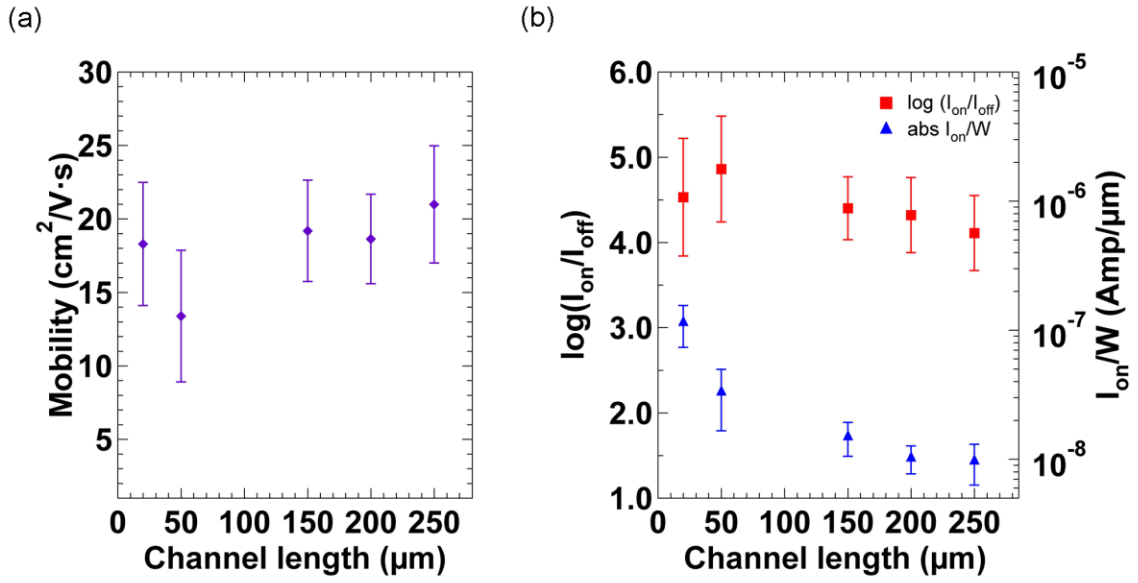

Figure 2.6: (a) Channel length dependence of the intrinsic mobility of the inkjet printed SWCNT TFTs. (b) Channel length dependence of log (I_{on}/I_{off}) and I_{on}/W of the inkjet printed SWCNT TFTs. Vertical error bars represent standard deviation of each device parameter. 375 devices in total (100 TFTs for L of 20, 50 and 150 μm, 50 TFTs for L = 200 μm, 25 TFTs for L = 250 μm) were fabricated and analyzed.

Intrinsic mobility, I_{on}/I_{off} and on current density (I_{on}/W) were measured in devices with different L (20, 50, 150, 200 and 250 μm). 375 TFTs in total were fabricated and measured for statistics. As shown in Figure 2.6(a), the mobility values are almost independent of L, which is consistent with negligible contact resistance deduced from characteristics shown in Figure 2.5(a). Most devices exhibit intrinsic mobility higher than 15 $cm^2 V^{-1} s^{-1}$ for various L. The highest intrinsic mobility we observed was 30.5 $cm^2 V^{-1} s^{-1}$ for bottom contact devices. Figure 2.6(b) shows log (I_{on}/I_{off}) and I_{on}/W as a function of L ($I_{on} = I_D$ at $V_{GS} = -5$ V and $V_{DS} = -0.5$ V). $I_{on}/I_{off} > 10^4$ was observed in most devices for various L. The highest I_{on}/I_{off} we observed was 7.4×10^6. The mobility we report in this work is more than an order of magnitude higher than the best reported values for TFTs

with inkjet printed conjugated polymers[31,32] and is also higher than those reported for inkjet printed metal oxides.[27,30]

2.4. CONCLUSION

We have demonstrated high performance SWCNT TFTs with mobilities exceeding 30 $cm^2 V^{-1} s^{-1}$ and low operating voltages by *single-pass* inkjet printing of SWCNTs on high-κ ZrO_2. The high mobilities achieved in this work show that sorted SWCNTs are a promising alternative to polymers and semiconducting oxides for inkjet printing-based fabrication. Surface energy modification of the ZrO_2 surface is the key to the realization of uniform and dense networks of SWCNTs. The *single-pass* inkjet printing process demonstrated in this chapter, combined with solution processed ZrO_2, shows great promise as a reliable and scalable method for high performance flexible electronics applications.

Chapter 3. Hybrid Complementary Circuits Based on Inkjet Printed Carbon Nanotubes and Zinc Tin Oxide*

3.1. INTRODUCTION

Complementary circuits utilize both n-channel and p-channel field-effect transistors (FETs), and possess many advantages over circuits with unipolar (exclusively p-channel or n-channel) transistors including lower power dissipation, higher noise margins, and ease of circuit design.[13] The goal of realizing printed complementary circuits, in which the active semiconductors, gate insulator and metal contacts are printed, is being pursued by many groups.[54-56] Such a technology will enable the fabrication of low-cost, large-area electronic circuits, which are expected to find applications in sensors, actuators, and other systems.[57-60] Much of the effort so far has focused on organic and polymeric semiconductor materials, many of which are solution processable.[54,56,59,60] More recently, other active materials such as amorphous oxides have emerged.[27-29,61] Several metrics such as mobility, on/off current ratio (I_{on}/I_{off}), sub-threshold swing, inverter switching speed and ring oscillator (ROSC) performance have been used to assess TFTs and integrated devices based on different materials. Among these metrics, the ROSC performance (i.e., speed, propagation delay/stage, and operating voltage) offers an avenue for a direct comparison of integrated circuits based on different materials while providing benchmarks and guidelines for future materials and process

*This chapter is based on References 52: Kim, B.; Jang, S.; Geier, M. L.; Prabhumirashi, P. L.; Hersam, M. C.; Dodabalapur, A. High-Speed, Inkjet-Printed Carbon Nanotube/Zinc Tin Oxide Hybrid Complementary Ring Oscillators. *Nano Lett.* **2014**, *14*, 3683–3687, and 53: Kim, B.; Geier, M. L.; Hersam, M. C.; Dodabalapur, A. Complementary D Flip-Flops Based on Inkjet Printed Single-Walled Carbon Nanotubes and Zinc Tin Oxide. *IEEE Electron Device Lett.* **2014**, *35*, 1245–1247. B.K. and A.D. designed the experiments. B.K. carried out fabrication and characterization of devices. S.J. helped with SWCNT inkjet printing. M.L.G., P.L.P., and M.C.H. provided semiconducting SWCNTs.

development.[62] We report, in this chapter, ROSCs with signal delay per stage of 140 ns, which is the fastest ROSC circuit with inkjet printed semiconductors to date. We emphasize that our circuits operate in air, indicating that such circuits are likely to possess good long-term operational stability.

For printed complementary circuits, leading materials choices for p-channel TFTs are conjugated polymers (particularly those based on donor-acceptor materials), small-molecule organic semiconductors, and sorted SWCNTs. The best polymer TFTs possess mobilities in the range of 4–10 $cm^2\ V^{-1}\ s^{-1}$,[32,63,64] although inkjet printed polymeric devices typically exhibit lower mobility values.[32,55] In the case of small molecule organic semiconductors forming crystalline films, it is possible to attain mobilities > 10 $cm^2\ V^{-1}\ s^{-1}$.[65,66] Typical n-channel TFT active materials choices are inorganic oxides,[27-29,61] polymeric and organic semiconductors,[67,68] SWCNTs that operate as ambipolar devices,[20,69] SWCNTs with an appropriate gate dielectric[70,71] or chemically doped SWCNTs.[72,73] In this chapter, ZTO was selected as the active semiconductor in the n-channel TFT due to its relatively high mobility[28,29] and air stability.[74] In many TFTs, the measured mobility is reduced when a local gate is patterned and the channel length is reduced.[64] Thus, comparisons of ROSC performance across different materials technologies assume even greater significance since the gates must be patterned for integrated circuits and the channel lengths have to be kept relatively small to achieve high operating speeds.

In this chapter, we report on the characteristics of complementary ROSCs and D flip-flops in which the p-channel TFTs active layer consist of a random network of sorted semiconducting SWCNTs[15,16,22] and the n-channel TFTs are based on amorphous ZTO.[28,29,61] Both these semiconductor materials are solution processable and can be readily deposited by inkjet printing. The gate insulator for both TFTs is ZrO_2, which is

deposited from solution by spin coating. Inkjet printed, high performance SWCNT[22] and oxide TFTs[27] have been individually reported in earlier work, but their direct integration into ROSCs or D flip-flops has not previously been achieved. Through the demonstration of the fastest ROSCs with inkjet printed semiconductors along with D flip-flops, we show that this combination of materials is among the best options for printed complementary circuits.

3.2. EXPERIMENTAL

3.2.1. Device fabrication

The gate patterns were defined on glass (SCHOTT Glass, Elmsford, NY, AF32eco) (for ROSCs) or Si/SiO_2 substrates (for D flip-flops) by photolithography, and Ti/Pt (3 nm/30 nm) was deposited using an e-beam evaporator, followed by lift-off. ZrO_2 dielectric layer was deposited by sequential spin coating and annealing. After ZrO_2 deposition, via holes to the gate electrodes were formed by photolithographic patterning and reactive ion etching with CHF_3/O_2 at a pressure of 40 mTorr. Following this step, the dielectric film was treated with UV O_3 for 15 min using a bench top UV cleaner (Novascan PSD-UVT) to promote the wetting of ZTO and SWCNT inks.[22] The preparation of ZTO and SWCNT inks are described in our previous papers.[22,29] The ZTO layers for n-channel TFTs were deposited using a FUJIFILM Dimatix 2800 printer in air.[74] After the printing of ZTO, the substrate was annealed on a hot plate at 500 °C for 1 h in air. SWCNT layers for p-channel TFTs were deposited using the same inkjet printer at room temperature in air. The concentration of SWCNTs in the ink was 0.75 mg mL^{-1}. The volume of each droplet was 10 pL, and the drop spacing was chosen to be 40 μm for both ZTO and SWCNT. After the printing of SWCNTs, the substrate was placed on a

hotplate at 200 °C for 30 min to remove residual solvents and surfactants. Finally, the S/D electrodes were patterned by photolithography, and Ti/Au (3 nm/50 nm) was deposited by thermal evaporation, followed by lift-off.

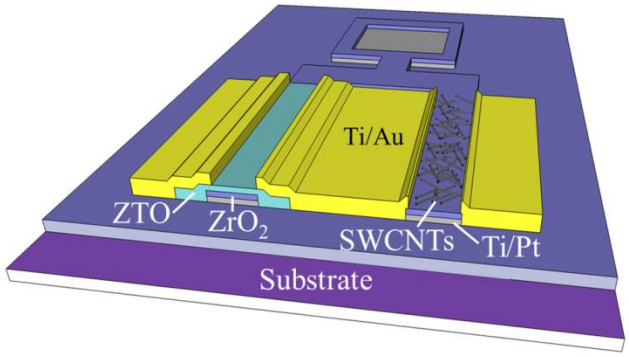

Figure 3.1: A schematic structure of an inkjet printed SWCNT (p-channel) and ZTO (n-channel) based inverter.

Figure 3.1 shows the schematic structure of the ZTO/SWCNT complementary inverter. A bottom-gate/top-contact device structure was employed for both n-channel and p-channel TFTs.

3.2.2. Electrical characterization of devices

All measurements were carried out in ambient conditions, attesting to the inherent reliability and stability of the materials systems. The characteristics of TFTs and inverters were measured with a HP 4155C semiconductor parameter analyzer. The ROSC measurements were performed with a LeCroy WaveRunner 6030 oscilloscope and a Tektronix AWG 2005 arbitrary waveform generator. The contact for the output signal of the ROSCs was made with a Picoprobe Model 12C.

For the measurement of the dynamic characteristics of the D flip-flops, the *Clock* (*CLK* and $\overline{CLK}$) and *Data* inputs were generated by a Tektronix AWG 2005 arbitrary waveform generator and V_{DD} and *GND* were supplied by the HP 4155C. The output

signal was measured with a Picoprobe Model 12C connected to a LeCroy WaveRunner 6030 oscilloscope.

3.3. RESULTS AND DISCUSSION

3.3.1. SWCNT and ZTO TFTs

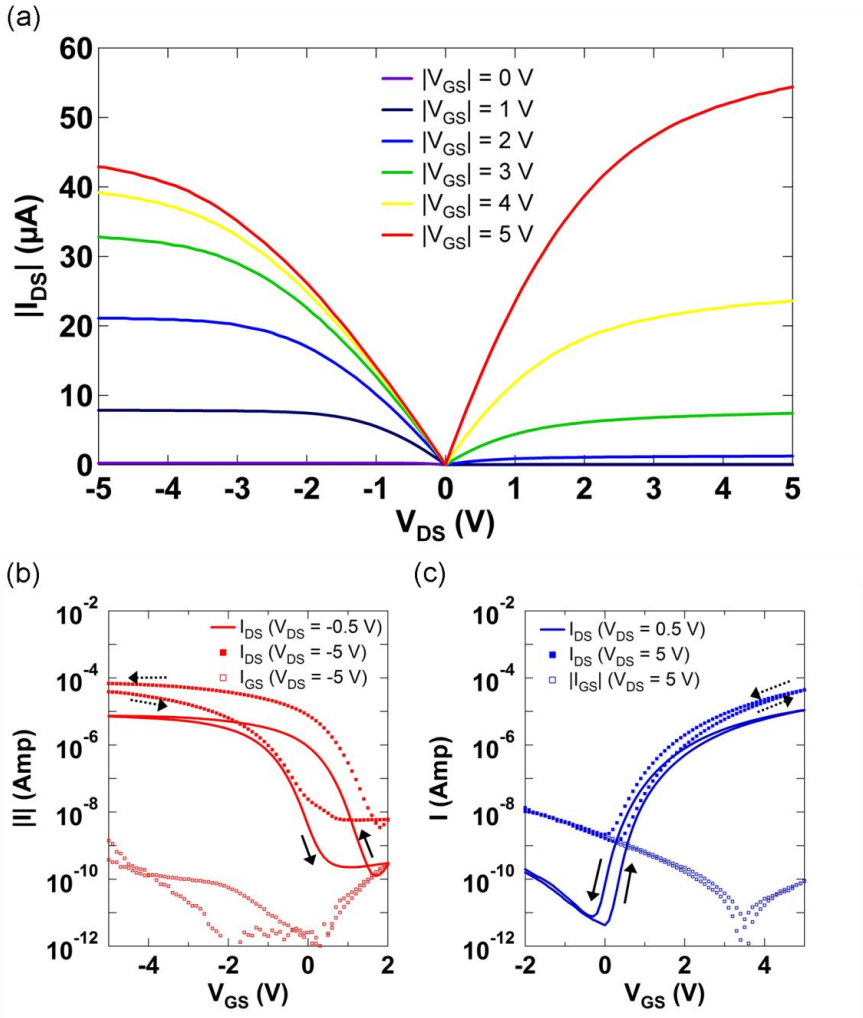

Figure 3.2: (a) Output characteristics of the inkjet printed SWCNT and ZTO TFTs (L=20 µm, W=400 µm). (b) Transfer characteristics of the inkjet printed SWCNT TFT (L=20 µm, W=400 µm). (c) Transfer characteristics of the inkjet printed ZTO TFT (L=20 µm, W=400 µm).

The electrical characteristics of SWCNT and ZTO TFTs with L = 20 μm and W = 400 μm are shown in Figure 3.2. The Ti/Au bilayer contact injects electrons and holes effectively for ZTO and SWCNT TFTs, respectively. The operating voltages for both TFTs are under 5 V due to the solution-processed high-κ dielectric with a capacitance per unit area of 148 nF cm^{-2}. The SWCNT TFT exhibits linear field-effect mobility (geometric mobility) of 1.7 $cm^2 V^{-1} s^{-1}$ at V_{DS} = −0.5 V, saturation field-effect mobility of 1.7 $cm^2 V^{-1} s^{-1}$ at V_{DS} = −5 V, and I_{on}/I_{off} of 3.2 × 10^4 at V_{DS} = −0.5 V (Figure 3.2(b)), while the ZTO TFT exhibits linear field-effect mobility of 4.1 $cm^2 V^{-1} s^{-1}$ at V_{DS} = 0.5 V, saturation field-effect mobility of 4.4 $cm^2 V^{-1} s^{-1}$ at V_{DS} = 5 V, and I_{on}/I_{off} of 2.6 × 10^6 at V_{DS} = 0.5 V (Figure 3.2(c)). We note that the calculated SWCNT TFT mobilities correspond to the geometric mobilities which differ from the intrinsic SWCNT mobilities. The intrinsic SWCNT mobilities depend upon the nanotube density and are typically at least a factor of 2 higher than the geometric mobility. A discussion of this issue and a detailed comparison between the two is reported in our previous work (Chapter 2.3).[22] The mobility values we measure in these devices are lower than those reported in ref. 22, because we used a lower concentration of SWCNTs in the ink solution to achieve lower power operation.

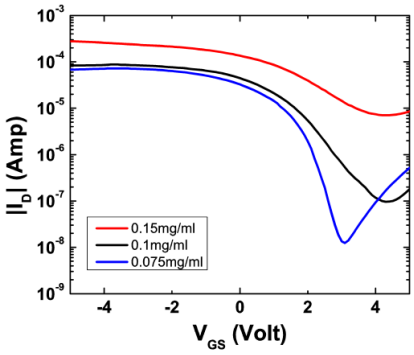

Figure 3.3: Transfer characteristics with various SWCNT ink concentrations (0.075, 0.1, and 0.15 mg mL^{-1}).

The effect of SWCNT ink concentration on a device performance was investigated for Si back-gate devices (Figure 3.3). TFTs with three different SWCNT ink concentrations (0.075, 0.1, and 0.15 mg mL^{-1}) were fabricated and measured. Both I_{on} and I_{off} increase as the SWCNT concentration increases; however, I_{off} is more sensitive to ink concentration. The device with 0.15 mg mL^{-1} concentration exhibits I_{on} (at $V_D = -0.5$ V), in the order of 100 µA, but I_{on}/I_{off} is less than 100. On the other hand, the device with 0.075 mg mL^{-1} concentration possesses I_{on} in the order of 10 µA and I_{on}/I_{off} of ~6000. This low I_{on}/I_{off} in the ink with high nanotube concentration can be explained by the nanotube screening effect in thick SWCNT films. The low concentration ink (0.075 mg mL^{-1}) was chosen in this study for low static power consumption, while higher concentration inks can be used for printed transistors in sub-circuits for which a high drive current capability is more important than a large I_{on}/I_{off}.

3.3.2. Inverter

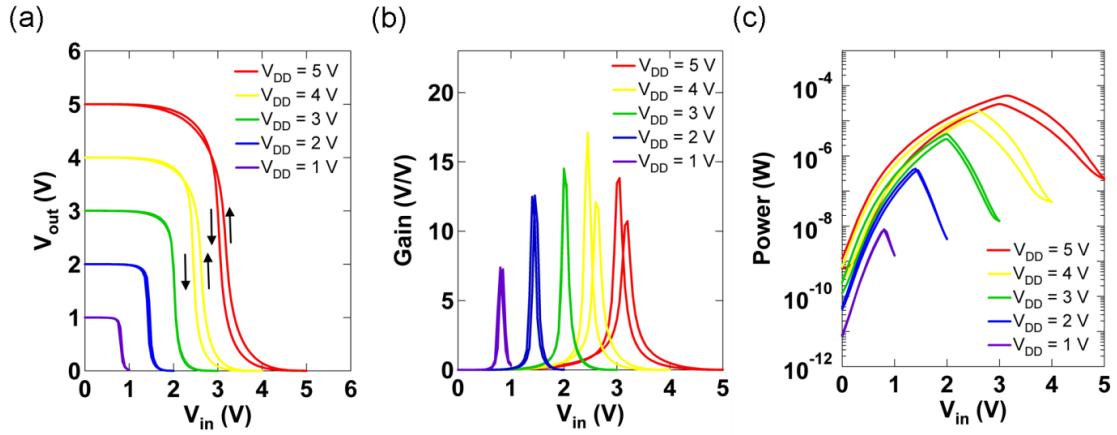

Figure 3.4: (a) VTCs of a complementary inverter at different supply voltages. (b) DC gain ($|dV_{OUT}/dV_{IN}|$) of the complementary inverter at different supply voltages. (c) Complementary inverter power consumption at different supply voltages.

The complementary inverter, composed of n-channel and p-channel TFTs, was demonstrated by connecting SWCNT (p-channel) and ZTO (n-channel) TFTs as shown in Figure 3.1. Figure 3.4(a) shows the voltage transfer characteristics (VTC) of the complementary inverter at different values of V_{DD} (1, 2, 3, 4, and 5 V). The complementary inverter possesses near rail-to-rail swing, good noise margins (NM_{HIGH} = 1.01 V, NM_{LOW} = 2.25 V when V_{DD} = 5 V, Figure 3.5), and high gain. Four important parameters of the inverter VTC are described in Figure 3.5; output high voltage (V_{OH}), output low voltage (V_{OL}), input high voltage (V_{IH}), and input low voltage (V_{IL}). High-input noise margin (NM_H) and low-input noise margin (NM_L) are defined as following equations: $NM_H = V_{OH} - V_{IH}$, $NM_L = V_{IL} - V_{OL}$.

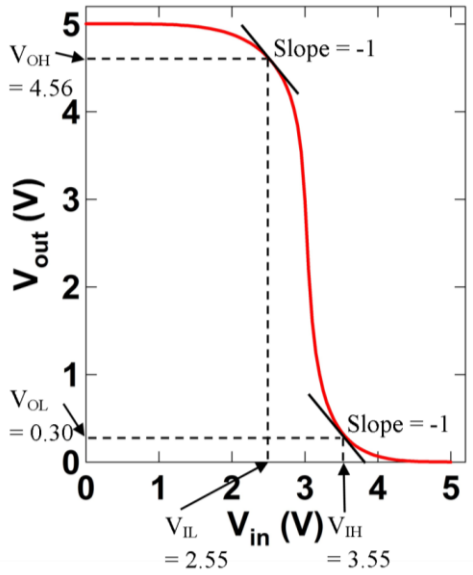

Figure 3.5: (a) Voltage transfer characteristic (VTC) of the complementary inverter at a supply voltage of 5 V and critical points.

The complementary inverter gains, defined as $|dV_{OUT}/dV_{IN}|$, at each V_{DD}, are shown in Figure 3.4(b). The maximum gain of 17.1 occurs at a V_{DD} of 4 V. Figure 3.4(c) shows the power consumption ($P = I_{SS}V_{DD}$) of the complementary inverter at different

supply voltages. The static power consumption when V_{IN} is HIGH or LOW was less than 0.25 μW at V_{DD} = 5 V. The power consumption at HIGH V_{IN} is several orders of magnitude higher than the power consumption at LOW V_{IN} as shown in Figure 3.4(c). This difference in power consumption is due to the SWCNT FET and ZTO FET having different off-current values at V_{GS} = 0 V. For HIGH V_{IN}, I_{SS} is equal to the current of the SWCNT FET at V_{GS} = 0 V (Figure 3.2(b)) while at LOW V_{IN}, I_{SS} is equal to the current of the ZTO FET at V_{GS} = 0 V (Figure 3.2(c)).

3.3.3. Ring oscillator

Five-stage ROSCs were fabricated by connecting five complementary inverters in a loop with a buffer stage in a circuit configuration as illustrated in Figure 3.6(a). The optical image of our ROSC is shown in Figure 3.6(b). The overlap between the gate electrode and S/D contacts were chosen to be 1 μm to reduce parasitic capacitances for high speed operation. Figure 3.6(c) displays the output signal of the ROSC with L = 4 μm and W = 80 μm for both n-channel and p-channel TFTs. This output signal shows near rail-to-rail swing, from V_{DD} to ground, with a relatively high oscillation frequency, which reaches 714 kHz at V_{DD} of 8 V. The signal delay per stage, t, was calculated from the equation: $t = 1/(2Nf)$, where N = 5 is the number of stages and f is the oscillating frequency. The minimum signal delay we measured was 140 ns at V_{DD} of 8 V.

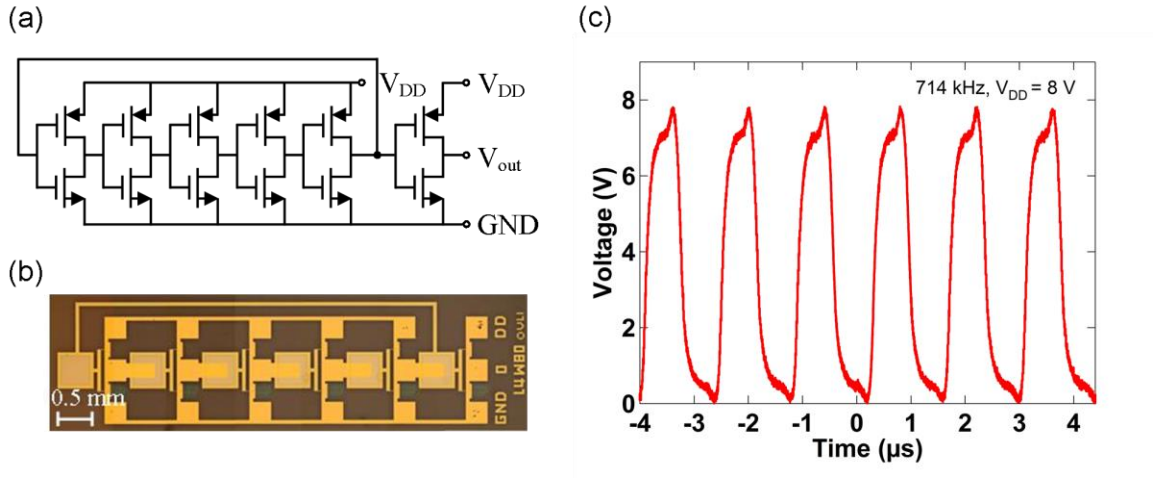

Figure 3.6: (a) Circuit diagram of a five-stage ROSC. The last stage is a buffer stage. (b) Optical micrograph of the five-stage ROSC. (c) The output signal of the ROSC. The oscillation frequency is 714 kHz at V_{DD} = 8 V.

The output signals of the complementary ROSCs at different V_{DD}s are shown in Figure 3.7. The oscillation frequency and the output swing of ROSCs increases as supply voltage (V_{DD}) increases. Even at a low operating voltage (V_{DD} = 4 V), the ROSC shows the oscillation frequency over 250 kHz.

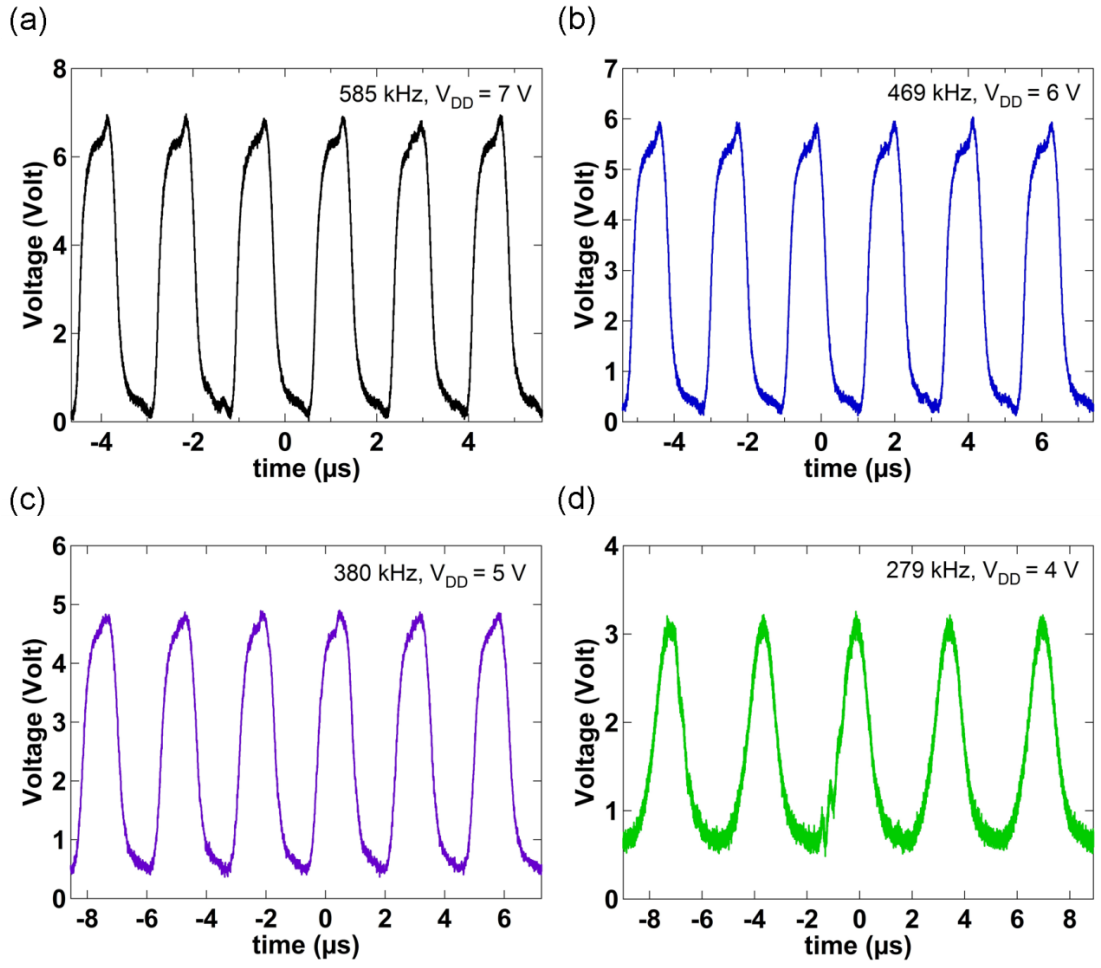

Figure 3.7: The output signals of the complementary ROSCs at different V_{DD}s. (a) V_{DD} = 7 V. (b) V_{DD} = 6 V. (c) V_{DD} = 5 V. (d) V_{DD} = 4 V.

The propagation delays per stage of our ROSCs as a function of V_{DD} are compared with those of some other reported ROSCs[20,75-78] in Figure 3.8. The ROSCs results we have chosen for comparison are the best reported results for TFT-based complementary and ambipolar ROSCs in which the active semiconductors are organic/polymeric semiconductors or oxide semiconductors.[75-78] Also included is the result based on random network SWCNT TFT ROSCs.[20] Our complementary ROSCs

compare favorably in terms of propagation delay and supply voltage. However, it should be noted that most of the referenced circuits (for comparison) utilize capital intensive vacuum processes to deposit semiconductor layers. To the best of our knowledge, our ROSC with signal delay per stage of 140 ns is the fastest ROSC circuit with printed semiconductors to date. Further improvement in the speed can potentially be achieved if smaller FET channel lengths are used. The complementary ROSCs have a shelf life (in N_2) of more than 6 months and operate continuously in air for more than 30 min with no passivation layer. With the use of passivation layers such as P(VDF-TrFE), the operating lifetime is expected to be very long.

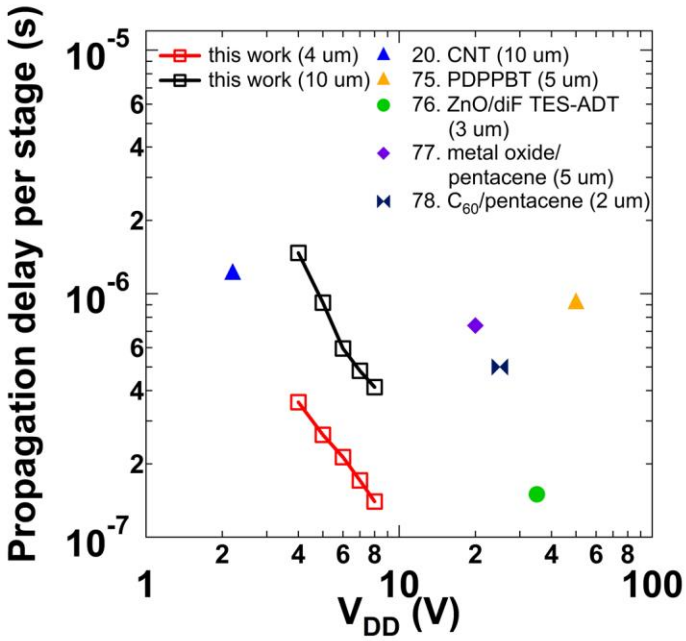

Figure 3.8: Propagation delay per stage of our ROSCs compared with other reported ROSCs as a function of supply voltage. The channel materials and channel lengths (in parenthesis) are indicated.

3.3.4. D flip-flop

Latches and flip-flops are the most commonly used building blocks in sequential

logic circuits such as decoders and memories. A latch is comprised of two transmission gates and two inverters, and a D flip-flop is constructed by combining two latches in series. A schematic diagram of the positive edge-triggered D flip-flop is shown in Figure 3.9(a). Figure 3.9(b) shows an optical microscope image of the complementary D flip-flop based on inkjet printed ZTO and SWCNTs. All 16 TFTs in the D flip-flop possess L = 20 μm and W = 400 μm.

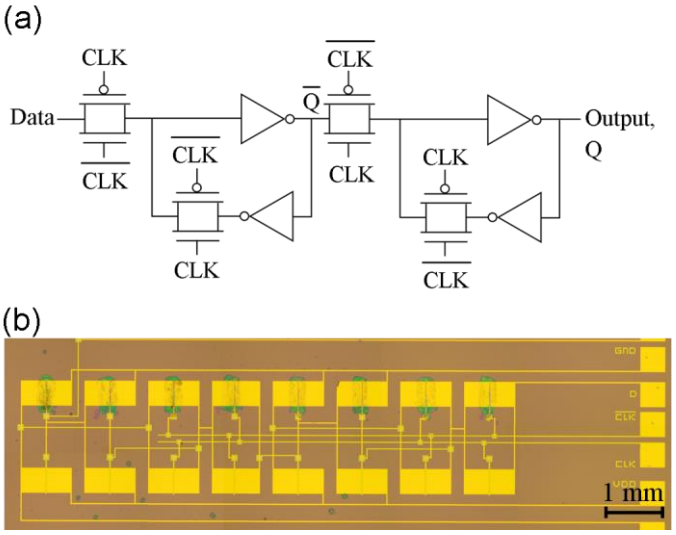

Figure 3.9: (a) Schematic of a pass transistor logic based positive edge-triggered D flip-flop. (b) Microscope image of the D flip-flop. Upper 8 TFTs are ZTO TFTs and lower 8 TFTs are SWCNT TFTs.

The positive edge-triggered D flip-flop samples the input data only at the rising edge of *CLK*. When *CLK* is LOW, the master latch becomes transparent and the input data (D) is inverted ($\overline{Q}$) at the end of the master latch, while the slave latch becomes opaque and holds previous data. When *CLK* is HIGH, the master latch becomes opaque and passes stored master value ($\overline{Q}$) regardless of D, while the slave latch becomes transparent and Q is measured at the output by inverting transmitted $\overline{Q}$.

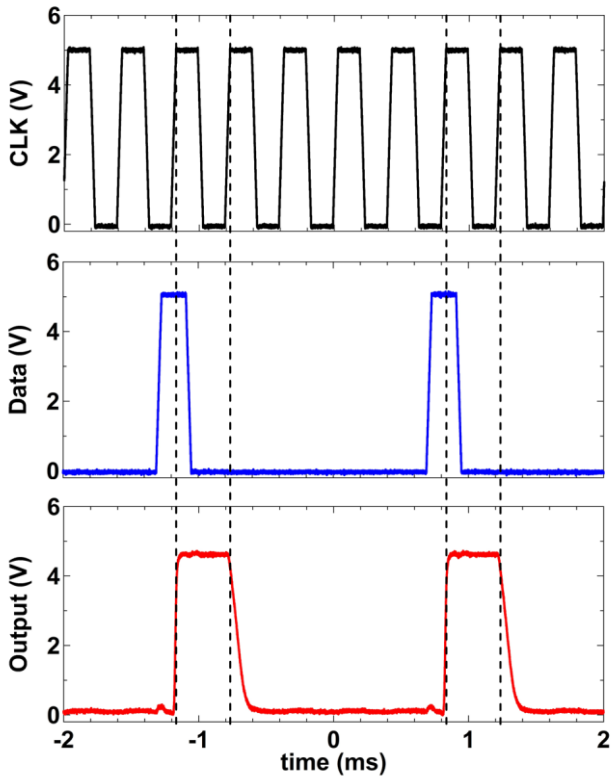

Figure 3.10: Measured output signal of the D flip-flop with *CLK* and *Data* inputs at a *CLK* frequency of 2.5 kHz.

The measured output signal of the D flip-flop is shown together with *CLK* and *Data* inputs in Figure 3.10. The D flip-flop based on inkjet printed ZTO and SWCNTs operates well at a *CLK* frequency of 2.5 kHz at V_{DD} of 5 V. This circuit operates well at a high *CLK* frequency under a low supply voltage, considering that both semiconductors are inkjet printed (Table 3.1).

Five-stage ROSCs with the same channel dimensions were also fabricated for comparison. The ROSCs show oscillation frequencies of ~20 kHz at V_{DD} = 5 V. The typical *CLK* frequencies of pass transistor logic based D flip-flops are lower than the oscillation frequencies of five-stage ROSCs.[79]

Table 3.1: Comparison of key metrics of TFT-based clocked circuits with printable semiconductors.

Ref.	n-type	p-type	CLK freq. (Hz)	Voltage (V)	L (μm)	Semiconductor deposition
This work	ZTO	SWCNT	2.5 k	5	20	Inkjet printing
80	-	SWCNT	50	−5	100	Filter Film Transfer
81	-	SWCNT	20	−5 to +5	170	Gravure printing
82	PDI-8CN2	P3HT	1.6 k	100	7.5	Printing
83	-	P3HT	5	−1.5	25	Aerosol-jet printing
84	-	TIPS-PEN:PS	-	10	5	Inkjet printing
85	Organic (unknown)		100	20	35	Inkjet printing
86	PTVPhI-Eh		20	60	20	Spin-coating

3.4. CONCLUSION

We have demonstrated a complementary circuit technology that can operate in air with inkjet printed SWCNT TFTs (p-channel) and amorphous ZTO TFTs (n-channel). Complementary inverters and five-stage ROSCs with superior performance have been demonstrated. The inverter gains are >15 and ROSC frequencies reach 714 kHz, the fastest for any ROSCs utilizing printed semiconductors. The D flip-flop operates at a *CLK* frequency of 2.5 kHz with low operating voltages (5 V) in ambient conditions. This promising combination of materials offers a significant leap in performance compared to previous thin-film based complementary circuits as well as a viable route for high-performance large-area complementary circuits produced by low cost printing techniques.

Chapter 4. Double-Gate Voltage-Controlled Ring Oscillators*

4.1. INTRODUCTION

One of the important application areas for printed electronics is in sensor systems.[1,88] In such systems, shown schematically as a block diagram in Figure 4.1, typically weak signals from a sensor are first amplified and then converted to digital form before being transmitted to external electronics. Thus, analog to digital signal conversion is a key functional block for printed electronics. Voltage-controlled oscillators (VCOs) are key components of VCO-based analog-to-digital converters (ADCs).[89,90] There have been a few reports on organic transistor based ADCs,[91-95] however, most of these were not based on printed semiconductors. In this chapter, we report the realization of voltage-controlled double-gate complementary ROSCs utilizing inkjet printed semiconductors.

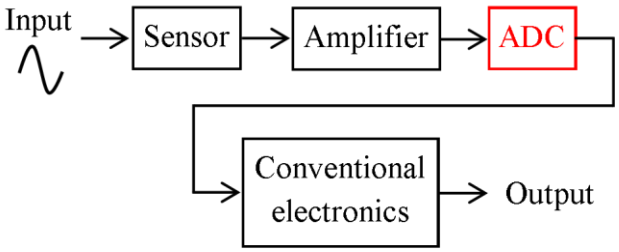

Figure 4.1: Schematic block diagram of a sensor system.

Numerous semiconductor and dielectric materials systems are being investigated for printed electronics. Semiconductor materials such as polymers, amorphous oxides,

*This chapter is based on Reference 87: Kim, B.; Park, J.; Geier, M.; Hersam, M. C.; Dodabalapur, A. Voltage-Controlled Ring Oscillators Based on Inkjet Printed Carbon Nanotubes and Zinc Tin Oxide. *ACS Appl. Mater. Interfaces* **2015**, *7*, 12009–12014. B.K. and A.D. designed the experiments. B.K. carried out fabrication and characterization of devices. J.P. helped with the basic circuit simulation. M.L.G. and M.C.H. provided semiconducting SWCNTs.

and SWCNTs have been demonstrated in printed electronics with each material possessing advantages and drawbacks for specific applications.[19,30,55,56,96,97] In previous work (Chapter 3), we demonstrated complementary circuits with inkjet printed p-channel SWCNT TFTs and n-channel amorphous oxide TFTs as foundational elements for printed electronics.[52,53] In this chapter, we show that the addition of double-gate functionality yields VCOs that are more easily implemented with printed transistors compared to traditional designs based on analog components such as operational amplifiers. Frequency tuning characteristics of double-gate ROSCs with a pentacene active layer have been previously reported.[98,99] However, their use in ADCs and the linearity of tuning characteristics have not received adequate attention and can be improved by using different semiconductors. The response of an ADC is governed by its bandwidth which is determined by the sampling rate. For systems such as those depicted in Figure 4.1, it is not necessary to implement a full ADC at the site of a sensor; rather, the focus should be on keeping the sampling rate as high as possible. This goal is best achieved with voltage-controlled ring oscillators (VCROs) that possess higher oscillation frequencies than the clock frequency of the corresponding digital circuits. Thus, a scheme in which the analog signal is converted to a frequency modulated square wave will efficiently propagate the signal from the sensor to the control electronics, where additional processing can be performed. Adding a buffer amplifier (i.e., two inverters in series) will improve the pulse shape of the VCO output, if required.

4.2. EXPERIMENTAL

4.2.1. Device fabrication

The bottom gate electrodes, which consist of patterned e-beam evaporated Ti/Pt bilayers (3 nm/30 nm), were formed on Si/SiO_2 substrates by photolithography, followed by lift-off. The bottom gate dielectric layer, ZrO_2, was deposited by a sol-gel route. Via holes to the bottom gate electrodes were patterned by photolithography and reactive ion etching (CHF_3/O_2 at a pressure of 40 mTorr). The n-type active layer, ZTO, was deposited by sequential inkjet printing three times, after UV O_3 surface treatment for 10 min. After ZTO printing, the substrate was annealed on a hot plate at 500 °C for 1 h in air. The p-type active layer, SWCNTs (>98% semiconducting purity prepared by DGU),[15,16] was deposited by inkjet printing, after UV O_3 surface treatment for 10 min. After printing the SWCNTs, the substrate was placed on a hot plate at 200 °C for 30 min in air to remove residual solvents. More details on preparation of ZrO_2, ZTO, and SWCNT solutions, and the printing conditions are described in our previous papers.[22,29,52,74] The S/D electrodes were patterned by photolithography, and Ti/Au (3.5 nm/20 nm) was deposited by thermal evaporation, followed by lift-off.

Poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) (Solvay Solexis Inc., 75/25 mol%) solution, dissolved in diethyl carbonate (25 mg/ml), was spin-coated on top of the devices at a spin speed of 2000 rpm for 45 s. The substrate was baked on a hot plate at 140 °C for 3 min in air to remove solvents. A thin Al_2O_3 layer (12.5 nm) was deposited on top of the P(VDF-TrFE) layer by atomic layer deposition (ALD) at 80 °C. After Al_2O_3 deposition, the top gate dielectrics on contact pads were removed with acetone. Finally, Ni (50 nm) was deposited by thermal evaporation through a shadow mask to form the top gate electrodes.

4.2.2. Electrical characterization of devices

All measurements were performed under ambient conditions. The characteristics of TFTs and inverters were measured using a HP 4155C semiconductor parameter analyzer. For the ROSC measurement, the output signals were measured with a LeCroy WaveRunner 6030 oscilloscope, and other voltages were supplied by the HP4155C.

4.3. RESULTS AND DISCUSSION

4.3.1. Double-gate SWCNT and ZTO thin-film transistors

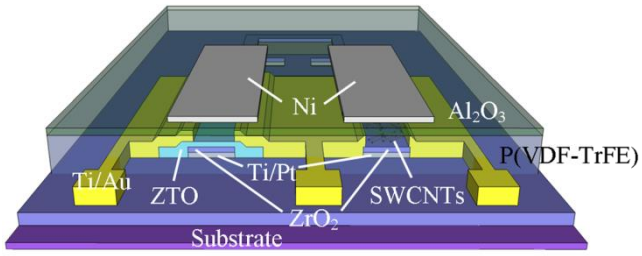

Figure 4.2: Schematic structure of a double-gate complementary inverter based on inkjet printed SWCNTs and ZTO.

Figure 4.2 illustrates a schematic structure of the double-gate complementary inverter based on inkjet printed SWCNTs and ZTO. The top gate dielectric for these devices consists of a bilayer of P(VDF-TrFE) and Al_2O_3. The P(VDF-TrFE) layer has been shown in previous work to mitigate the effects of charged defects in the p-channel SWCNTs, leading to significantly improved electrical characteristics.[100] A thin Al_2O_3 layer was deposited on top of the P(VDF-TrFE) to reduce gate leakage current and improve the overall gate dielectric stack performance.

The threshold voltage (V_{th}) of the TFTs in a double-gate structure can be controlled by the potential applied to either the bottom or top gate.[101-105] In this chapter,

bottom gates were employed as conventional gates (as in single gate TFTs) because the bottom gate dielectric exhibits a higher capacitance value (148 nF cm^{-2}) than that of the top gate dielectric (~106 nF cm^{-2}) (Figure 4.3), while the top gates were employed as the control gates. Metal (Ti/Au)-insulator (P(VDF-TrFE)/Al_2O_3)-metal (Ni) capacitors were fabricated with the TFTs in order to measure the capacitance-voltage characteristics of the top gate dielectric (Figure 4.3).

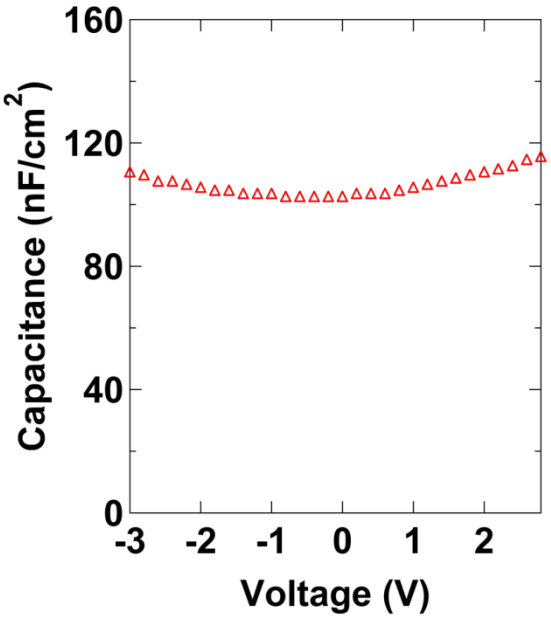

Figure 4.3: Capacitance-voltage characteristics of a bilayer of P(VDF-TrFE)/Al_2O_3 at 1 kHz.

Figure 4.4(a) and (b) show transfer characteristics of the double-gate TFTs in linear mode ($|V_{DS}|$ = 0.5 V). Both ZTO and SWCNT TFTs possess the same L = 20 µm and W = 400 µm. The ZTO TFT exhibits linear field-effect mobility of 0.7 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} of 8.5×10^2, while the SWCNT TFT exhibits linear field-effect mobility of 0.3 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} of 6.2×10^3, when n-TFT top gate-source voltage ($V_{GS}^{T,n}$) and p-TFT top gate-source voltage ($V_{GS}^{T,p}$) are 0 V, and $|V_{DS}|$= 0.5 V. In the case of the ZTO

TFT, V_{th} shifts toward more negative voltage and I_{on} increases when $V_{GS}^{T,\,n}$ increases. In the case of the SWCNT TFT, V_{th} shifts toward more positive voltage and $|I_{on}|$ increases when $V_{GS}^{T,\,p}$ decreases. Figure 4.4(c) and (d) show output characteristics of the double-gate TFTs at both $V_{GS}^{T,\,p}$ and $V_{GS}^{T,\,n}$ = 1.5 V, and at both $V_{GS}^{T,\,p}$ and $V_{GS}^{T,\,n}$ = −1.5 V, respectively. I_{DS} varies depending on V_{GS}^{T} for both TFTs, however, the difference in I_{DS} between when V_{GS}^{T} = 1.5 V and V_{GS}^{T} = −1.5 V is smaller in the SWCNT TFT compared to the ZTO TFT. This difference can be attributed to the lower gate modulation of the SWCNT TFT in saturation regime (Figure 4.5). A possible reason for this is that the top gate dielectric stack is thicker for SWCNT TFTs compared to ZTO TFTs.

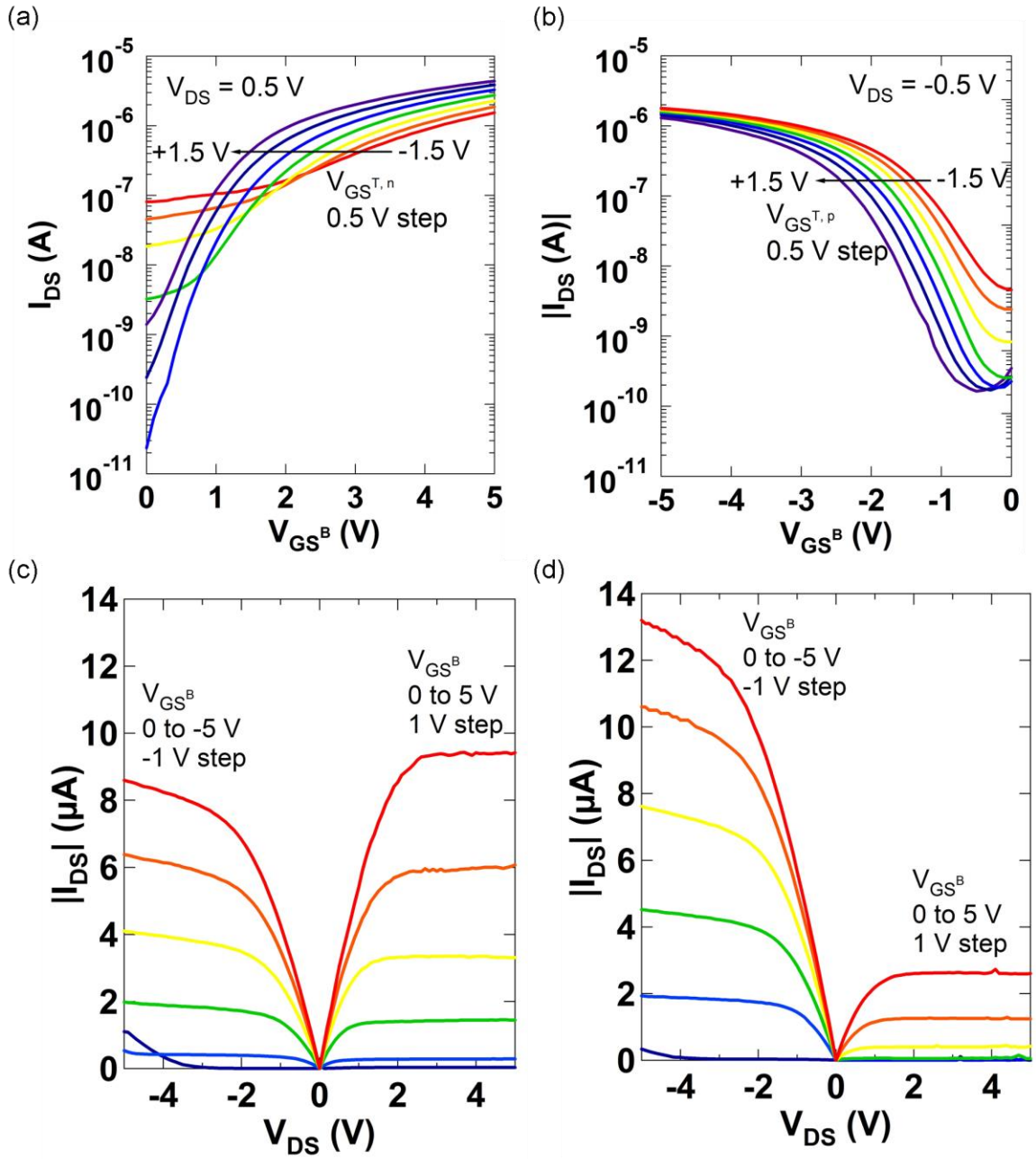

Figure 4.4: (a) Transfer characteristics of the double-gate ZTO TFT at various n-TFT top gate-source voltages ($V_{GS}^{T,n}$). (b) Transfer characteristics of the double-gate SWCNT TFT at various p-TFT top gate-source voltages ($V_{GS}^{T,p}$). (c) Output characteristics of the double-gate SWCNT (left) and ZTO (right) TFTs at V_{GS}^{T} = 1.5 V, and (d) at V_{GS}^{T} = −1.5 V.

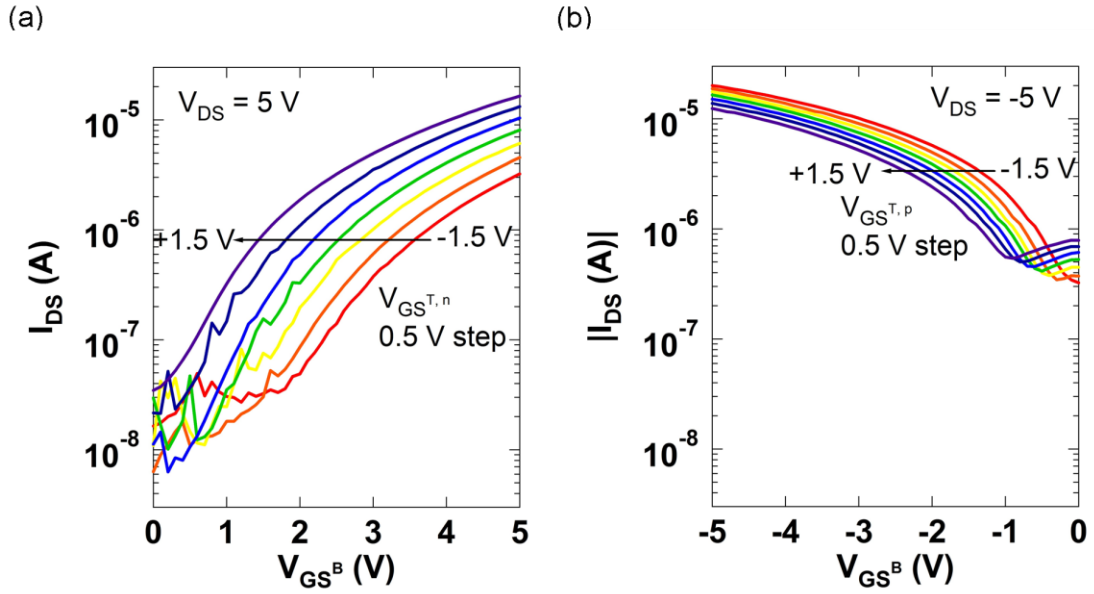

Figure 4.5: (a) Transfer characteristics of the double-gate ZTO TFT at various n-TFT top gate-source voltages ($V_{GS}^{T, n}$) when V_{DS} = 5 V. (b) Transfer characteristics of the double-gate SWCNT TFT at various p-TFT top gate-source voltages ($V_{GS}^{T, p}$) when V_{DS} = −5 V.

4.3.2. Double-gate inverter

A complementary inverter was constructed by connecting double-gate SWCNT (p-channel) and ZTO (n-channel) TFTs as illustrated in Figure 4.2 and the insets of Figure 4.6(a) and (b). The inverter was characterized by applying V_{GS}^{T} to either top gate of the p-TFT or n-TFT, while the other top gate was connected to its source. Input voltages (V_{IN}) were applied to the connected bottom gate. Figure 4.6(a) shows voltage transfer characteristics of the inverter at different $V_{GS}^{T, n}$, where the curve shifts to the left along the axis of V_{IN} when $V_{GS}^{T, n}$ increases. This shift occurs because I_{DS} of the n-TFT increases with the increase of $V_{GS}^{T, n}$, while I_{DS} of the p-TFT remains same. DC gains ($|dV_{OUT}/dV_{IN}|$) of the inverter at different $V_{GS}^{T, n}$ are shown in Figure 4.6(c). The maximum gain point also shifts to the left when $V_{GS}^{T, n}$ increases. These shifts are

observed similarly when $V_{GS}^{T,\,p}$ increases (Figure 4.6(b) and (d)). In this case, $|I_{DS}|$ of the p-TFT decreases with the increase of $V_{GS}^{T,\,p}$, while I_{DS} of the n-TFT remains same. However, the shifts are less in magnitude in the SWCNT TFT case for the reason mentioned in Chapter 4.3.1.

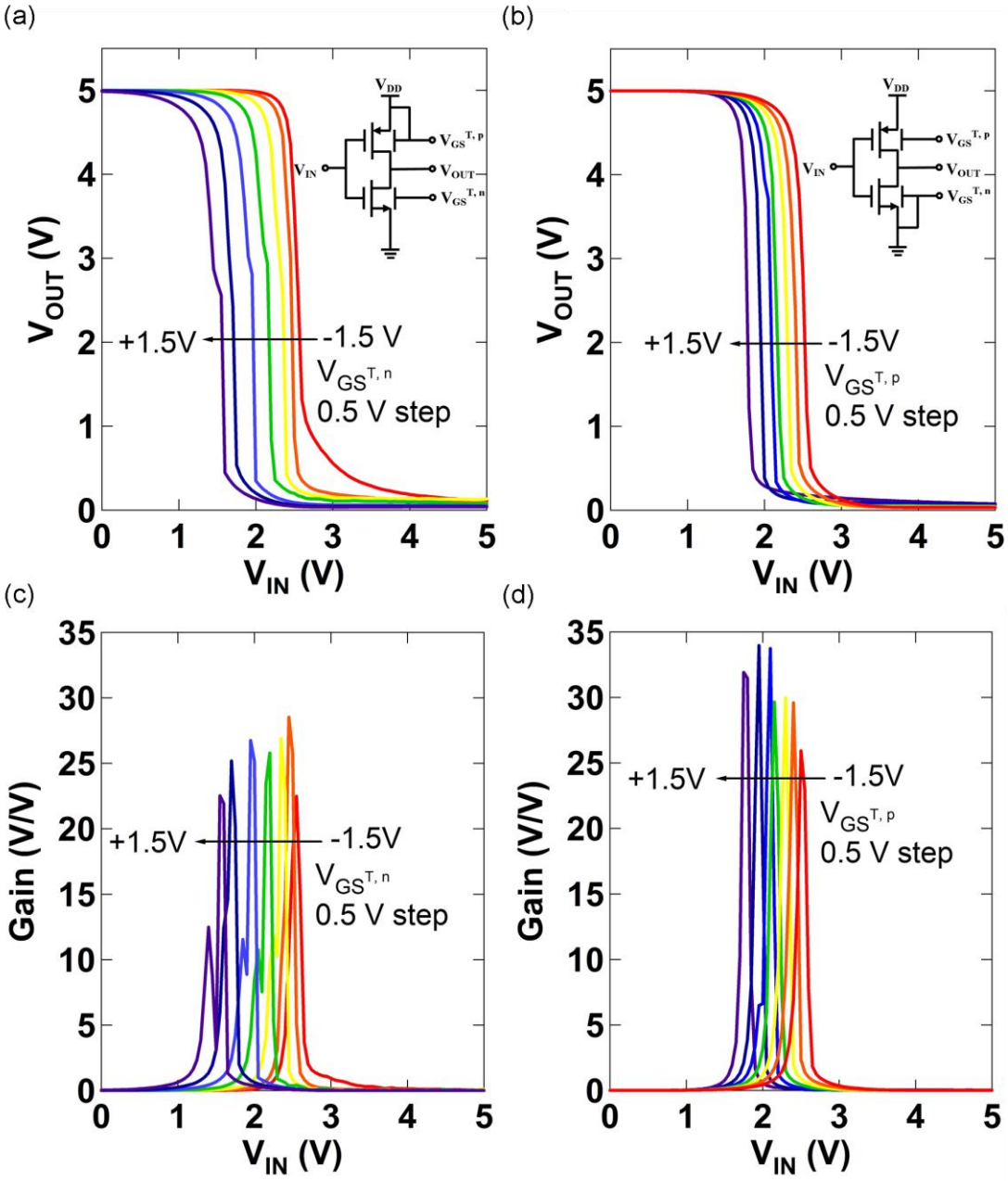

Figure 4.6: (a) Voltage transfer characteristics (VTC) of the double-gate complementary inverter as a function of $V_{GS}^{T, n}$ and (inset) the top gate of p-TFT connected to source (V_{DD}) of p-TFT. (b) DC gains ($|dV_{OUT}/dV_{IN}|$) of the inverter as a function of $V_{GS}^{T, n}$. (c) VTC of the double-gate complementary inverter as a function of $V_{GS}^{T, p}$ and (inset) the top gate of n-TFT connected to source (GND) of n-TFT. (d) DC gains of the inverter as a function of $V_{GS}^{T, p}$.

4.3.3. Double-gate ring oscillator

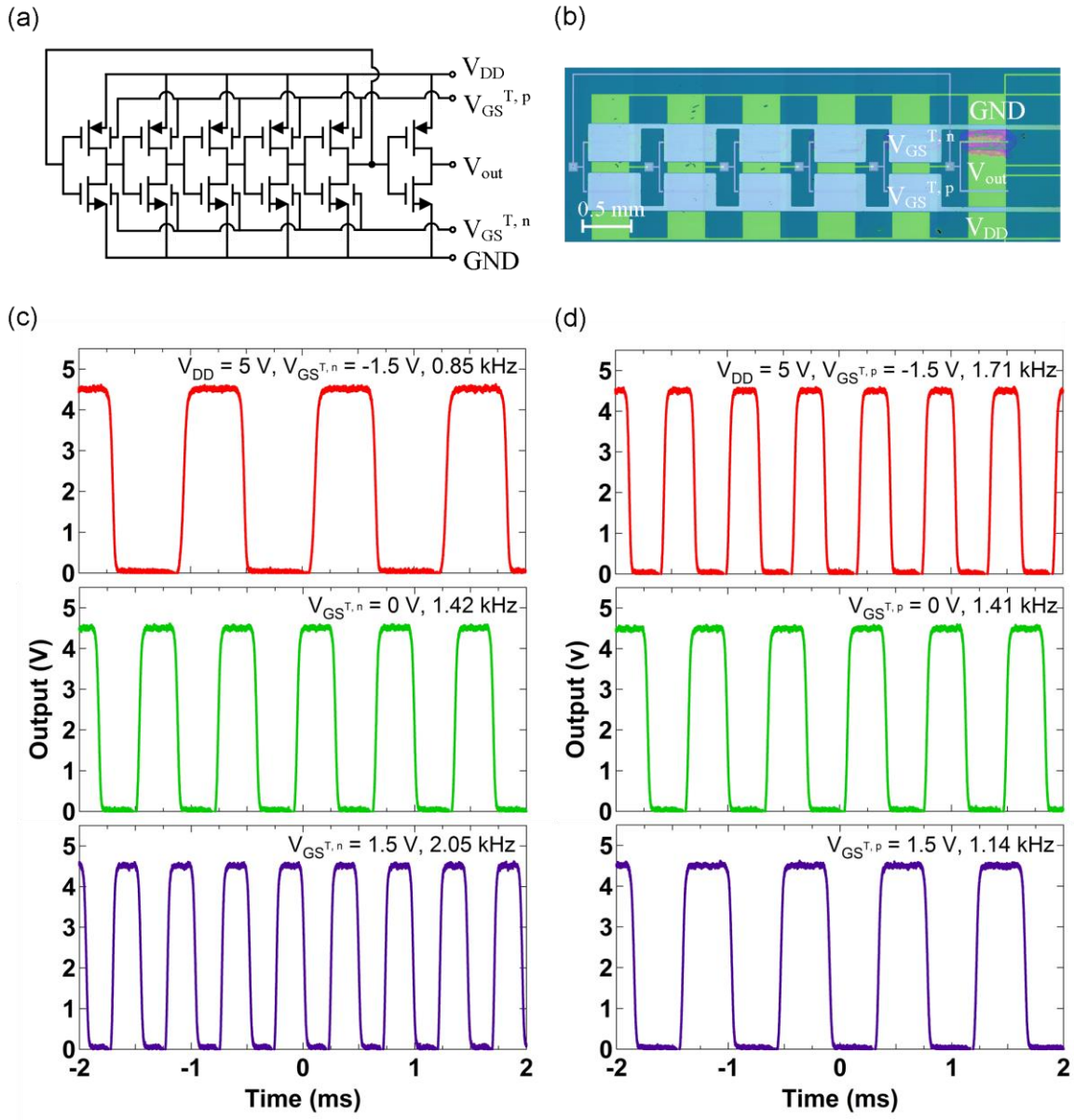

Figure 4.7: (a) Circuit diagram of a double-gate five-stage ROSC. (b) Optical micrograph of the double-gate five-stage ROSC. The upper 6 TFTs are ZTO (n-channel) TFTs and the lower 6 TFTs are SWCNT (p-channel) TFTs. (c) Output signals of the double-gate ROSC at different $V_{GS}^{T,n}$, and (d) at different $V_{GS}^{T,p}$.

The double-gate V_{th} tuning characteristics can be applied to ROSC circuits to control their oscillation frequencies. For example, five double-gate inverters were connected in a loop to construct a five-stage double-gate ROSC with a buffer stage as shown in Figure 4.7(a). Figure 4.7(b) shows an optical micrograph of the ROSC. All TFTs in the ROSC circuit possess the same channel dimensions (L = 20 µm, W = 400 µm). Figure 4.7(c) and (d) show output signals of the ROSC at three different $V_{GS}^{T, n}$ and $V_{GS}^{T, p}$, respectively, resulting in a frequency modulation of the ROSC. In particular, the oscillation frequency of the ROSC increases as $V_{GS}^{T, n}$ increases (Figure 4.7(c)). In contrast, the oscillation frequency of the ROSC decreases as $V_{GS}^{T, p}$ increases (Figure 4.7(d)).

Figure 4.8 shows propagation delay per stage of the double-gate ROSC as a function of $V_{GS}^{T, n}$ (Figure 4.8(a)) and $V_{GS}^{T, p}$ (Figure 4.8(b)) at V_{DD} = 5 V. The propagation delay per stage of the ROSC was calculated from the equation $t = 1/(2Nf)$, where $N = 5$ is the number of stages and f is the oscillation frequency.

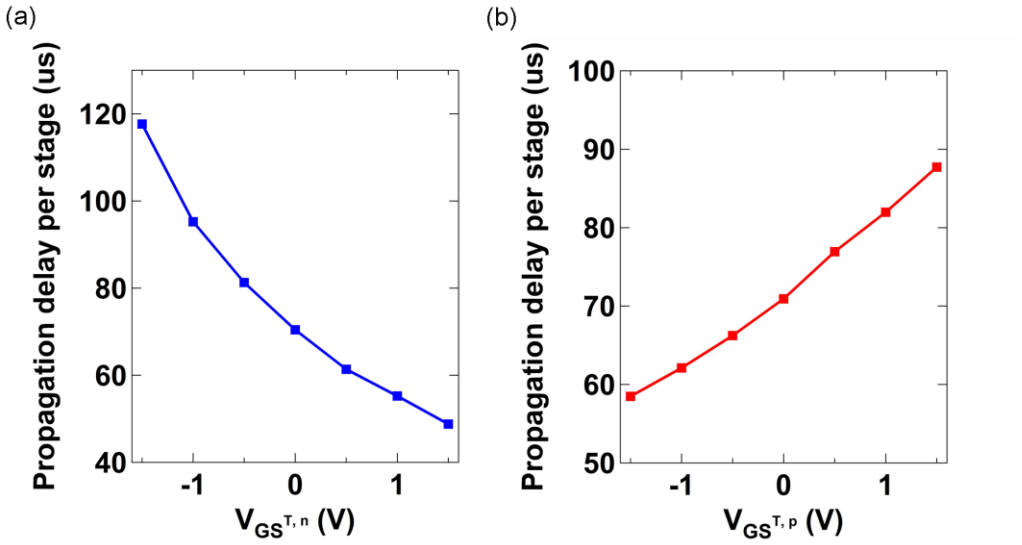

Figure 4.8: Propagation delay per stage of the double-gate ROSC as a function of top gate-source voltages of (a) n-TFTs, and (b) p-TFTs.

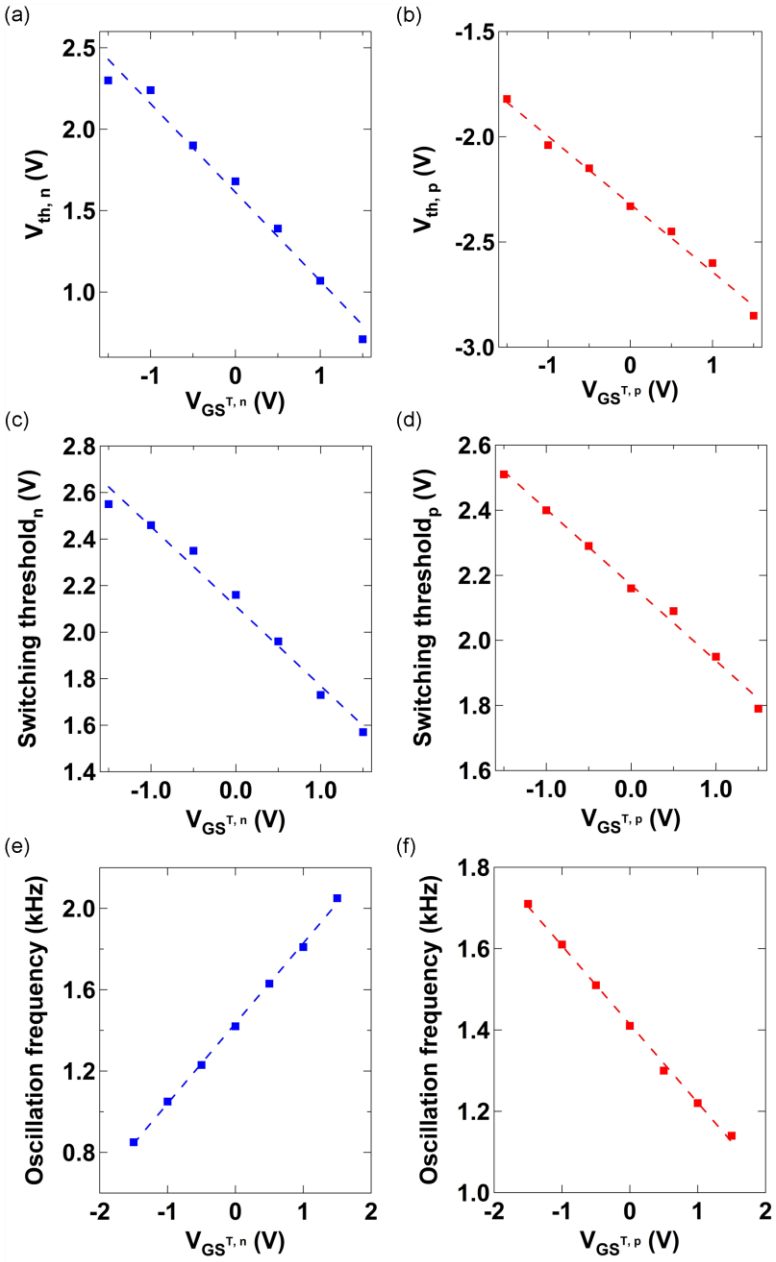

Figure 4.9: (a) Threshold voltage shift of the ZTO TFT as a function of $V_{GS}^{T,n}$. (b) Threshold voltage shift of the SWCNT TFT as a function of $V_{GS}^{T,p}$. (c) Switching threshold shifts of the inverter as a function of $V_{GS}^{T,n}$ and (d) as a function of $V_{GS}^{T,p}$. (e) Oscillation frequencies of the double-gate ROSC as a function of $V_{GS}^{T,n}$ at V_{DD} = 5 V and (f) as a function of $V_{GS}^{T,p}$ at V_{DD} = 5 V. Dotted lines in (a)–(e) show linear fitting of the measured data (shown in squares).

Figure 4.9 shows summarized tuning characteristics of the top gate potentials on TFTs, inverters, and ROSCs. Figure 4.9(a) shows the V_{th} tuning characteristics of the ZTO TFT by applying different $V_{GS}^{T,\ n}$, and Figure 4.9(b) shows the V_{th} tuning characteristics of the SWCNT TFT by applying different $V_{GS}^{T,\ p}$. The switching threshold of the inverter, where $V_{IN} = V_{OUT}$, decreases when $V_{GS}^{T,\ n}$ and $V_{GS}^{T,\ p}$ increases (Figure 4.9(c) and (d)).

The frequency of the ROSC increases linearly as $V_{GS}^{T,\ n}$ increases (Figure 4.9(e)), while the frequency decreases linearly as $V_{GS}^{T,\ p}$ increases (Figure 4.9(f)). Quantitatively, linear fitting curves almost exactly match the measured data points ($R^2 = 0.999$ in Figure 4.9(e), $R^2 = 0.997$ in Figure 4.9(f)). This linearity is expected from the basic equation (eq 4.1)) that describes the oscillation frequency in a CMOS-based ROSC:[106]

$$f \propto \frac{1}{NR_{on}C} \propto V_{th} \qquad \text{(eq 4.1)}$$

where N is the number of stages, R_{on} is the on-resistance, C is the capacitance. Such a linear characteristic will result in minimal distortion of the analog signal. The frequency modulated square wave output of the VCRO will have a higher bandwidth (and hence sampling rate) compared to a conventional ADC,[91-93] in which the slow clock speeds of the organic or printed electronics based digital electronics will limit performance. This improvement occurs because the oscillation frequencies of ROSCs are typically much higher than the clock frequencies of flip-flops or other digital components for any given technology.

4.4. CONCLUSION

A VCRO has been demonstrated by employing a double-gate structure where the active semiconductors of the circuits are deposited by inkjet printing. Threshold voltages in individual TFTs, switching thresholds in complementary inverters, and oscillation frequencies in ROSCs are systemically controlled by applying top gate-source voltages in double-gated devices. A key requirement for the VCO, linearity between frequencies and voltages, has been achieved by simply adding a top gate dielectric and top gates on top of conventional ROSCs in place of more complex circuit designs. Consequently, the circuits demonstrated here are likely to accelerate efforts to realize printed electronics based signal processing in distributed sensors and related technologies.

Chapter 5. Ambipolar Transistors and Circuits Based on Carbon Nanotubes/Zinc Tin Oxide Heterostructures*

5.1. INTRODUCTION

Ambipolar TFTs have received significant attention due to their unique operation, which allows both electrons and holes to be injected and transported depending on the gate bias in a single device. These devices can operate in a dominantly unipolar mode or in an ambipolar mode.[107,108] The former mode is useful in logic devices, whereas the latter mode has been useful in light emitting devices.[109,110] Ambipolar TFTs based on organic semiconductors have been experimentally realized with different active layer configurations including bilayer,[107,108] blend,[111] and single-component[63,112,113] configurations. Organic-inorganic hybrid field-effect device architectures, which employ an organic semiconductor for hole transport and an inorganic oxide semiconductor for electron transport have also been reported.[114-116] In this chapter, we demonstrate the operation of hybrid ambipolar transistors, inverters, and ROCSs in which the active semiconductor consists of a bilayer of semiconducting SWCNTs and amorphous ZTO.

Sorted SWCNTs (semiconducting purity > 98%) have been recently shown to result in high performance TFTs[16,22,36,56,72,117-119] with mobilities in excess of 30 $cm^2\ V^{-1}\ s^{-1}$ and large on/off current ratios (> 10^5),[16,22,36] and are promising materials for printed electronics due to their solution processability as well as superior electrical, mechanical,

*This chapter is based on References 52: Kim, B.; Jang, S.; Geier, M. L.; Prabhumirashi, P. L.; Hersam, M. C.; Dodabalapur, A. High-Speed, Inkjet-Printed Carbon Nanotube/Zinc Tin Oxide Hybrid Complementary Ring Oscillators. *Nano Lett.* **2014**, *14*, 3683–3687, and 74: Kim, B.; Jang, S.; Geier, M. L.; Prabhumirashi, P. L.; Hersam, M. C.; Dodabalapur, A. Inkjet Printed Ambipolar Transistors and Inverters Based on Carbon Nanotube/Zinc Tin Oxide Heterostructures. *Appl. Phys. Lett.* **2014**, *104*, 062101. B.K. and A.D. designed the experiments. B.K. carried out fabrication and characterization of devices. S.J. helped with SWCNT inkjet printing. M.L.G., P.L.P., and M.C.H. provided semiconducting SWCNTs.

chemical properties.[10,11] Furthermore, SWCNTs have been shown to exhibit ambipolar behavior with appropriate processing and under inert measurement conditions.[19,20,69,120] However, SWCNT TFTs typically exhibit substantially unipolar (p-type) transport under ambient conditions due to adsorption of oxygen and moisture.[10,11] Amorphous metal oxide based FETs, which display primarily n-type characteristics, have been shown in recent studies to possess high carrier mobilities (>10 $cm^2\ V^{-1}\ s^{-1}$). ZTO is one of the promising amorphous metal oxide semiconductors and can be conveniently deposited from solution precursors as well as using vacuum based approaches. Amorphous ZTO has been shown to possess n-type behavior with mobility values in excess of 25 $cm^2\ V^{-1}\ s^{-1}$.[5,29,121]

Herein, we report high performance inkjet printed ambipolar TFTs, inverters, and ROSCs based on a heterostructure of ZTO and SWCNTs. SWCNTs are inkjet printed (p-channel) on top of the inkjet printed ZTO film (n-channel) to enable ambipolar transport. We make use of bilayer Ti/Au electrodes, which facilitate the injection of both carriers without large injection barriers. The bottom gated ambipolar TFTs exhibit carrier mobilities exceeding 2 $cm^2\ V^{-1}\ s^{-1}$, for both holes and electrons under ambient conditions. We further demonstrate complementary-like inverters with high gain and the fastest ambipolar ROSCs by integrating these ambipolar TFTs.

5.2. EXPERIMENTAL

Figure 5.1(a) shows the schematic structure of the inkjet printed heterostructure ambipolar TFT. Figure 5.1(b) shows the optical image of an inverter circuit based on TFTs possessing W = 1000 μm and L = 50 μm. Two layers of high-κ ZrO_2 dielectric (thickness 90–100 nm) were deposited on a heavily doped Si wafer (which was employed

as the gate) using a sol-gel route.[48] The dielectric surface was exposed to UV light in air for 10 min, causing the surface to become more hydrophilic, facilitating the deposition of the ZTO layer. The ZTO layer was deposited by inkjet printing on a ZrO_2 dielectric using a FUJIFILM Dimatix 2800 printer in air. The cartridges employed in ZTO and SWCNT printing were designed for 10 pL drop volume. The diameters of each droplets on UV O_3 treated ZrO_2 were 90 μm for ZTO drop and 70 μm for SWCNT drop. The drop spacings were chosen to be 40 μm for both ZTO and SWCNT printing. To ensure adequate thickness of the ZTO layer (30–40 nm), the inkjet printing of the ZTO solution was repeated 4 times. The substrate temperature during printing was maintained at 60 °C.[122] Following inkjet printing, the substrate was annealed on a hotplate at 500 °C for 1 h in air to facilitate the conversion of the ZTO precursor film to amorphous ZTO, as described previously.[29,48] After annealing, the source and drain electrodes consisting of a bilayer of Ti (3 nm) and Au (50 nm) were patterned by photolithography and lift-off. Next, the surface of ZTO film was exposed to UV light in air for 10 min to promote the wetting of the SWCNT ink.[22]

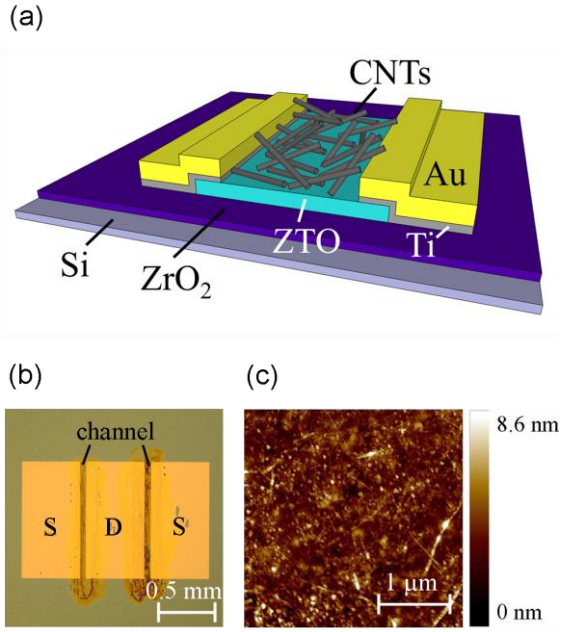

Figure 5.1: (a) Schematic device structure of the inkjet printed heterostructure ambipolar TFT. (b) Optical image of heterostructure ambipolar TFTs (L = 50 μm, W = 1000 μm). (c) AFM image of the inkjet printed channel layers.

The SWCNT ink was synthesized by dispersing >98% semiconductor purity SWCNTs (P2 arc discharge SWCNTs from Carbon Solutions), as determined by UV-Vis spectroscopy, in CHP at a concentration of 0.75 mg mL^{-1}. This ink was then inkjet printed on UV O_3 treated ZTO film at room temperature in air. Finally, the substrate was dried on a hotplate at 200 °C for 30 min in air to remove residual solvent. Figure 5.1(c) shows the AFM image of the inkjet printed channel layers. In the fabricated device, the ZTO TFT utilizes top contacts while the SWCNT TFT utilizes bottom contacts. A detailed description on the preparation of ZTO and semiconducting SWCNT inks are described in our previous work.[22,29,48]

For ambipolar TFT-based inverters (with local gate electrodes) and ROSCs, the gate patterns and via holes were defined by the same process as described in Chapter 3.2.1. A P(VDF-TrFE) film was deposited on top of the devices.

The electrical characteristics of both TFTs and inverters were measured in ambient conditions using a HP 4155C semiconductor parameter analyzer. The ROSC measurements were performed as described in Chapter 3.2.2.

5.3. RESULTS AND DISCUSSION

5.3.1. Bilayer ambipolar thin-film transistors

Figure 5.2 shows the output (I_{DS}-V_{DS}) and transfer (I_{DS}-V_{GS}) characteristics of a bilayer heterostructure ambipolar TFT. The operating voltage is less than 5 V due to the relatively thin high-κ ZrO_2 dielectric. In Figure 5.2(a), the linear operation regime (at low drain voltage, V_{DS}) shows no significant barriers to carrier injection for either electrons or holes, indicating good charge carrier injection efficiency of Ti/Au bilayer contacts for both (ZTO and SWCNT) transport layers. A typical characteristic of ambipolar TFTs is a diode-like behavior at low gate voltage (V_{GS}) with high V_{DS} due to the injection of significant density of "minority" carriers (electrons at $V_{DS} < 0$ V and holes at $V_{DS} > 0$ V). The transfer characteristics were measured at both negative (Figure 5.2(b)) and positive V_{DS} (Figure 5.2(c)). The symmetric "V-shape" is a consequence of balanced current levels for similar voltage magnitudes in the field-controlled diode and FET modes of operation.

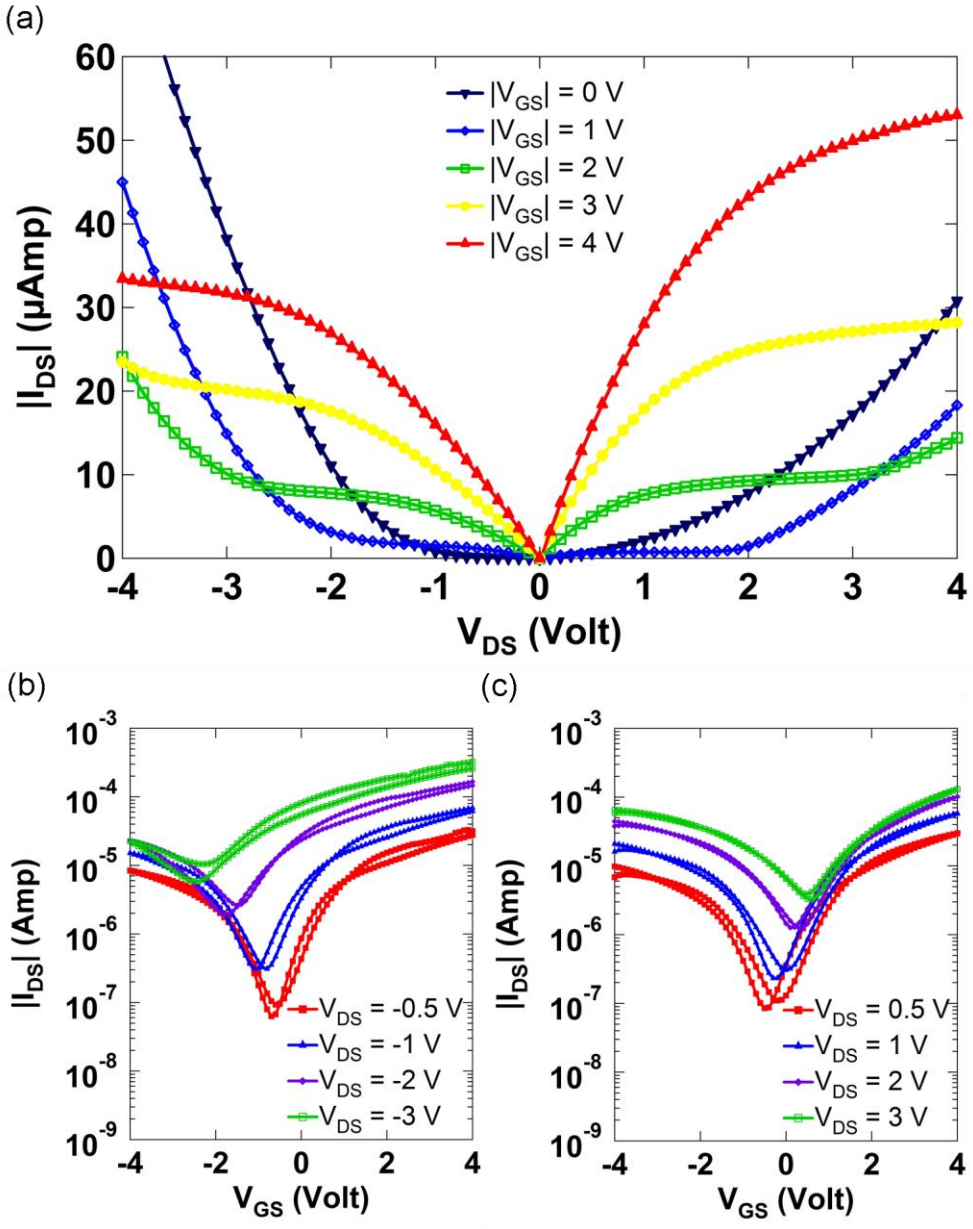

Figure 5.2: (a) Output (I_{DS}-V_{DS}) characteristics of the inkjet printed heterostructure ambipolar TFT (L = 150 μm, W = 3000 μm). (b) Transfer (I_{DS}-V_{GS}) characteristics of the the same device at different negative drain voltages and (c) at different positive drain voltages.

The hole and electron mobilities were calculated to be 2.4 ± 0.8 and 5.1 ± 2.5 cm^2 V^{-1} s^{-1} for p- and n-channel accumulation-mode operation, respectively, from 40 TFTs

possessing different channel lengths (L of 20, 50, 150, 200, and 250 μm, W/L = 20). The highest hole and electron mobilities we obtained were 4.2 and 11.5 $cm^2\ V^{-1}\ s^{-1}$, respectively. These mobility values were extracted from the equation (eq 5.1):

$$\mu = \frac{L}{W} \times \frac{1}{C_{ox}} \times \frac{1}{V_{DS}} \times \frac{dI_{DS}}{dV_{GS}} \qquad \text{(eq 5.1)}$$

where μ is linear field-effect mobility, I_{DS} is the drain current, C_{ox} is the capacitance per unit area, W is the channel width, and L is the channel length. Specifically, C_{ox} was measured to be 160 nF cm^{-2}, $|V_{DS}|$ was 0.5 V. The width-normalized contact resistance,[123] calculated from devices with different channel lengths, is 9 kΩ-cm for p-channel operation and 18 kΩ-cm for n-channel operation for a gate voltage of 3 V. For calculating the hole mobility, we assumed a reduced capacitance per unit area due to the ~40 nm thick ZTO layer that is immediately above the ZrO_2. The standard deviation of the hole mobility of ambipolar FETs operated in the hole enhancement mode was slightly higher than that of unipolar FETs made with only SWCNT active layers.[22] We note that the hole mobilities we calculated are the geometric mobilities. Very often, in the CNT literature, the intrinsic mobility is listed. Intrinsic mobilities, which depend upon the number of nanotubes per unit channel width, are typically at least a factor of two higher than the geometric mobility. A discussion of this issue and a detailed comparison between the two is made in Chapter 2.3. A $\log_{10}(I_{on}/I_{off})$ of 2.9 ± 0.5 and 2.6 ± 0.4, a turn-on voltage (the voltage at the lowest I_{DS}) of 0.01 ± 0.31 and −0.02 ± 0.27 V, and a subthreshold swing of 0.71 ± 0.27 and 0.42 ± 0.16 V dec^{-1} were extracted from electron and hole enhancement mode operation, respectively.

Table 5.1: Comparisons of key metrics of representative ambipolar TFTs in the literature.

Ref.	n-mater.	p-mater.	μ_n ($cm^2\ V^{-1}\ s^{-1}$)	μ_p ($cm^2\ V^{-1}\ s^{-1}$)	Operating voltage (V)	Measurement condition
This work	ZTO	SWCNT	11.5	4.2	4	Air
112	DPPT-TT		1.56	1.36	100	N_2
113	PDPP-TBT		1.45	0.7	80	Vacuum
63	PTDPPSe-SiC5		4.34	8.84	100	N_2
120	SWCNT		unknown	unknown	5	Air
69	SWCNT		2.86	0.08	50	N_2
20	SWCNT		20	20	1.5	Vacuum
124	SnO		1.02	0.32	40	Air
114	IZO	Pentacene	13.8	0.14	80	Vacuum
115	ZnO	PTAA:diF-TESADT	2–4.5	1.6–2.4	80	Air
116	ZnO	Pentacene	0.38	0.34	80	Air

It is useful to compare the key performance metrics of ambipolar TFTs across different materials families. Table 5.1 summarizes the key metrics for different materials, which include the electron and hole mobilities (carrier density dependent), operating voltage, and the measurement environment. Many ambipolar transistors, particularly those based on semiconducting polymers, are typically operated under vacuum or in inert atmosphere. Many of these devices show severe degradation in performance under ambient conditions. Polymer based ambipolar FETs have made impressive strides in recent years, principally due to the emergence of donor-acceptor polymers with high mobilities.[63,112,113] For example, J. Lee *et al.* have recently reported electron and hole

mobilities of 4.34 and 8.84 $cm^2\ V^{-1}\ s^{-1}$, respectively (measured in N_2), for side-chain engineered conjugated, alternating electron donor-acceptor polymers.[63]

Similarly, there have been a few demonstrations of ambipolar FETs based on hybrid inorganic/organic heterostructures.[114-116] However, these hybrid oxide/organic ambipolar FETs typically suffer from imbalanced (larger electron mobility as compared to the hole mobility) mobilities due to sub-optimal charge injection for the organic (p-channel) semiconductor.[114] Among oxide semiconductors, SnO is the only material that exhibits ambipolar behavior with electron and hole mobilities ~1 $cm^2\ V^{-1}\ s^{-1}$.[124] SWCNTs have demonstrated high performance ambipolar behavior, with balanced mobilities of 20 $cm^2\ V^{-1}\ s^{-1}$ when combined with ion gel type gate dielectrics and measured in vacuum.[20] Ambipolar operation in SWCNTs in air with such large mobilities has not been reported yet, presumably due to enhancement in hole transport through atmospheric adsorbate doping effects.[10,11] Our approach of utilizing a hybrid SWCNT/oxide heterostructure, on the other hand, combines the preferred charge transport attributes of amorphous metal oxides (i.e., electron transport) and SWCNTs (i.e., hole transport). Such ambipolar TFTs can operate in air with high stability. This is illustrated in Figure 5.3 for devices with no passivation of any kind. These devices have the added advantage of compatibility with solution-based inkjet printing, which makes them attractive for large area, roll-to-roll, low-cost electronic applications.

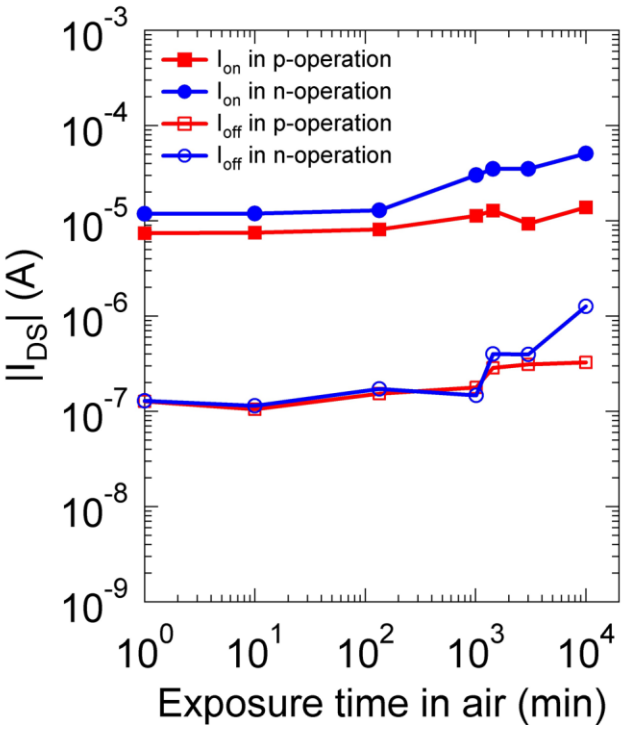

Figure 5.3: Air-stability of the inkjet printed heterostructure ambipolar TFT as a function of time.

5.3.2. Inverter based on bilayer ambipolar transistors

To demonstrate the utility of the ambipolar hybrid transistors, inverters (with a common Si gate) were realized by combining two identical TFTs (W = 3000 µm and L = 150 µm) in a circuit configuration shown as the inset in Figure 5.4(a). The input voltage (V_{IN}) was applied through a common Si substrate back-gate. In this inverter design, the power supply (V_{DD}) and ground terminals are interchangeable due to the device symmetry. Figure 5.4(a) shows a well-defined inverter operation at different values of V_{DD} (3 V and 5 V). The output voltage (V_{OUT}) is not constant for both high and low values of V_{IN}, where V_{OUT} increases slightly with V_{IN}. This common feature of ambipolar inverters arises because one of the TFTs is not completely turned off while the second

TFT is turned on. Similarly shaped voltage transfer curves were also measured at negative V_{IN} and V_{DD} as well. Figure 5.4(b) shows voltage gain, defined as $|dV_{OUT}/dV_{IN}|$. The complementary-like inverter exhibits maximum gain of 22.8 at V_{DD} of 3 V, which is more than sufficient for the construction of digital circuits. Ambipolar transistors can be employed as transmission gates in complementary circuits. Another possible use (in analog circuits) is as high-gain front end amplifiers as ambipolar inverters have demonstrated gains more than 100.[113]

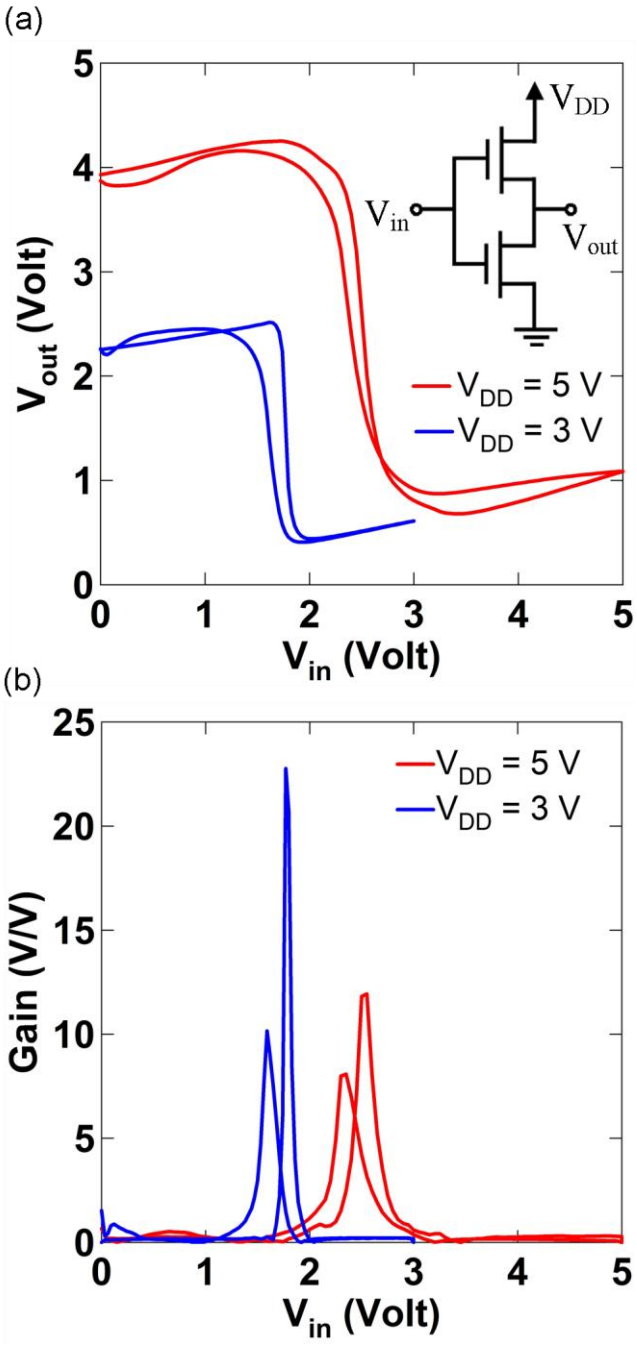

Figure 5.4: (a) Voltage transfer characteristics of a complementary-like inverter at different supply voltages. Inset shows a schematic of the electrical connections. (b) DC gain ($|dV_{OUT}/dV_{IN}|$) of the inverter at different supply voltages.

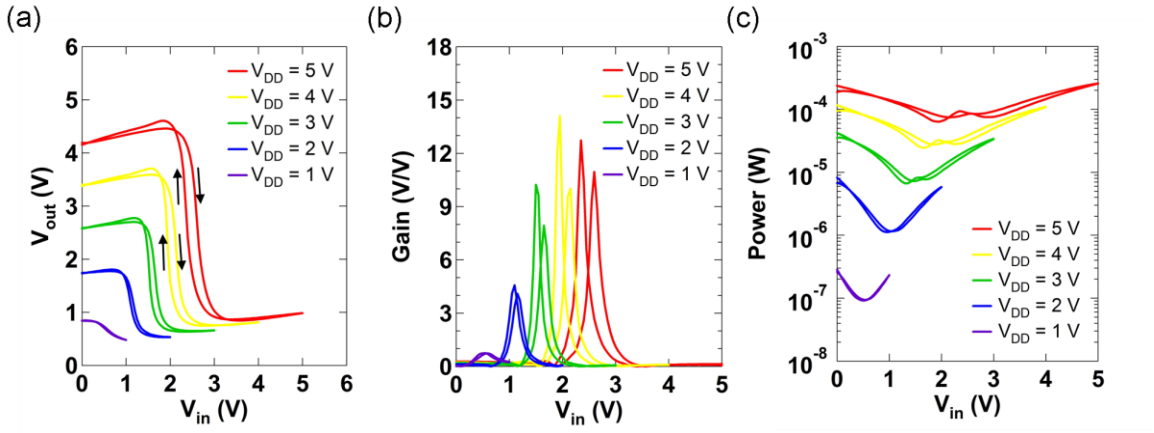

Figure 5.5: (a) VTCs of an ambipolar inverter at different supply voltages. (b) DC gain ($|dV_{OUT}/dV_{IN}|$) of the ambipolar inverter at different supply voltages. (c) Ambipolar inverter power consumption at different supply voltages.

Ambipolar inverters with local gate electrodes were also fabricated. Figure 5.5(a) shows the VTCs of the ambipolar inverter at different values of V_{DD}. The noise margins (NM_{HIGH} = 1.00 V, NM_{LOW} = 1.20 V when V_{DD} = 5 V, Figure 5.6) of the ambipolar inverter were lower than those of the complementary inverter (NM_{HIGH} = 1.01 V, NM_{LOW} = 2.25 V when V_{DD} = 5 V, Figure 3.5). The ambipolar inverter gains, as shown in Figure 5.5(b), are comparable to gains of the complementary inverter (Figure 3.4(b)). It can be seen in Figure 5.5(c) that the power dissipation in ambipolar inverters is significantly higher than in conventional complementary inverters (Figure 3.4(c)). This is due in large part to the nature of the current voltage characteristics of ambipolar transistors—none of the TFTs can be completely turned off.

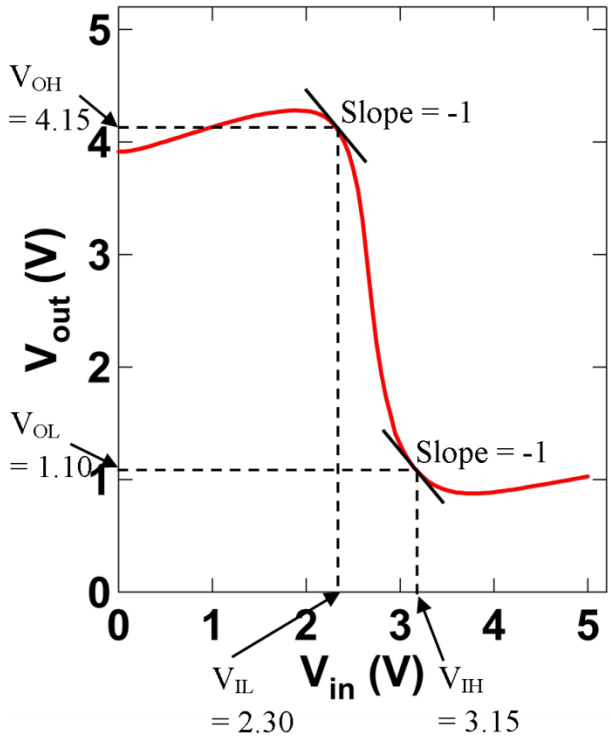

Figure 5.6: VTC of the ambipolar inverter at a supply voltage of 5 V and critical points. $NM_H = V_{OH} - V_{IH}$, $NM_L = V_{IL} - V_{OL}$.

5.3.3. Ring oscillator based on bilayer ambipolar transistors

Five-stage ROSCs were also realized using ambipolar transistors. The oscillator characteristics are shown in Figure 5.7. The overlap between the gate electrode and S/D contacts were 2 µm, and the ambipolar FETs used in these ROSCs have L = 20 µm and W = 400 µm. The oscillation frequencies for conventional (in Chapter 3.3.3) and ambipolar ROSCs appear comparable for the same supply voltage and when corrected for channel length differences. The oscillation amplitude of conventional ROCSs is higher than that of the ambipolar ROSCs and approaches the supply voltage (Figure 3.6(c)). The reduced oscillation amplitude of ambipolar ROSCs is due to their inverter characteristics which do not have rail-to-rail swings and which possess smaller noise margins. P(VDF-

TrFE) was added as a cap layer to improve device stability and uniformity for the ambipolar ROSCs.

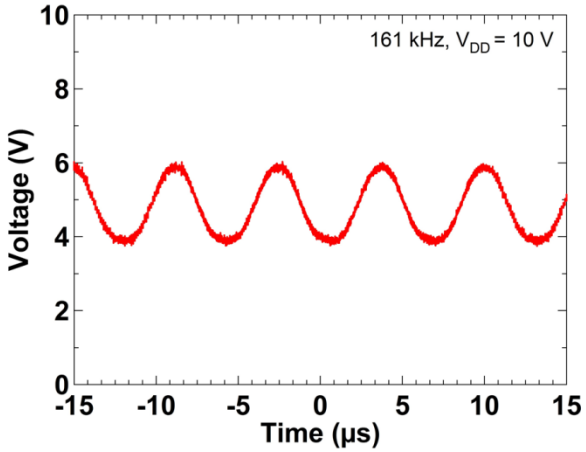

Figure 5.7: The output signal of the ROSC based on bilayer ambipolar TFTs.

The output signals of the ambipolar ROSCs at different V_{DD}s are shown in Figure 5.8. The oscillation frequency and the output swing of ROSCs increases as supply voltage (V_{DD}) increases.

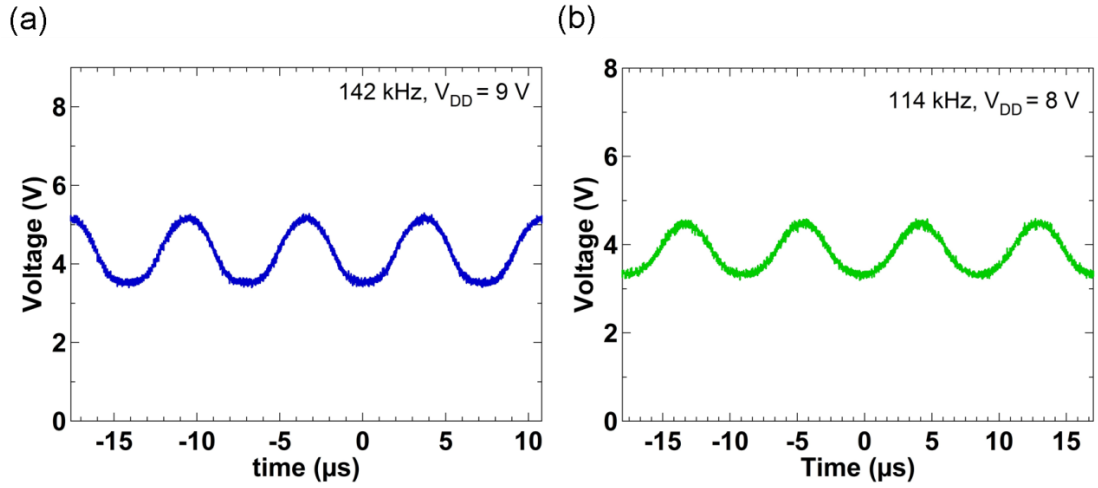

Figure 5.8: The output signals of the ambipolar ROSCs (a) at V_{DD} = 9 V and (b) at V_{DD} = 8 V.

The propagation delays per stage of ambipolar ROSCs as a function of V_{DD} are also compared with those of some other reported ROSCs in Figure 5.9. To the best of our knowledge, our ambipolar TFT-based ROSC is the fastest ROSC among any kind of ambipolar TFT-based ROSCs.

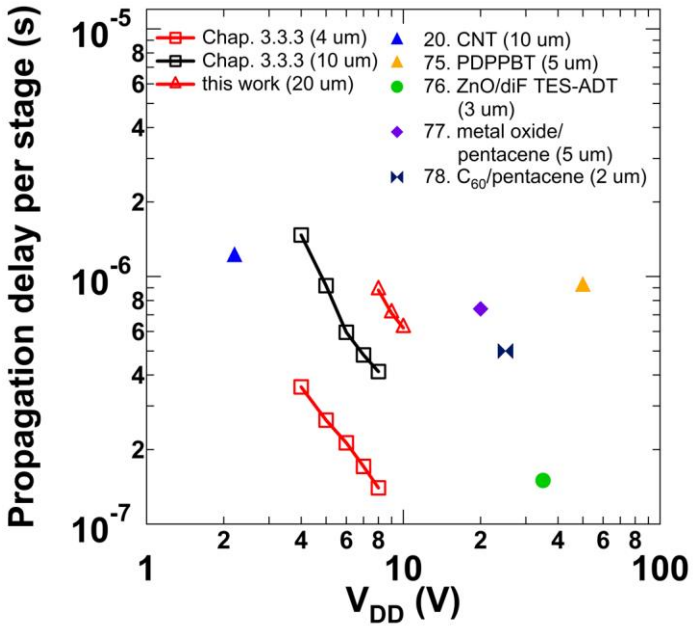

Figure 5.9: Propagation delay per stage of the ambipolar ROSC compared with other reported ROSCs as a function of supply voltage. The channel materials and channel lengths (in parenthesis) are indicated. Triangular symbols in three different colors indicate results from ROSCs based on ambipolar TFTs.

5.4. CONCLUSION

We have demonstrated ambipolar TFTs, inverters, and ROSCs based on bilayer heterostructures of ZTO and SWCNTs by inkjet printing. The bilayer heterostructures of ZTO and SWCNTs facilitate ambipolar transport in bottom gate device structures with solution-deposited high-κ gate dielectrics in ambient atmosphere. These ambipolar

heterosturuture TFTs exhibit balanced and high hole and electron mobilities exceeding 2 $cm^2\ V^{-1}\ s^{-1}$ with low operating voltages. Inverters composed of two identical ambipolar TFTs show clear signal inverting operation with a high gain of 22.8. ROSCs comprised of bilayer ambipolar transistors demonstrate the fastest oscillation frequency among previously reported ambipolar ROSCs. These results suggest that inkjet printed ambipolar heterostructure TFTs are promising candidates for realizing solution processable, high performance, large area advanced logic devices.

Chapter 6. Carbon Nanotube Ambipolar Transistors and Circuits on Flexible Substrates*

6.1. INTRODUCTION

Printing technologies are currently of great interest in the fabrication of electronics. Various printing techniques, which are traditionally utilized in media and art work, have been transformed into sophisticated device fabrication methods for low-cost, large-area, and flexible electronics. Numerous electronic functional materials have been deposited by printing and have been successfully integrated into functional electronic applications.[62,126,127] Among those materials, semiconducting SWCNTs have attracted a great deal of attention as an active material in TFTs due to their superlative charge transport characteristics, optical transparency, and chemical and mechanical properties.[12,18,128] Although SWCNTs are intrinsically ambipolar materials, they ordinarily exhibit predominantly unipolar p-type conduction under ambient conditions.[10,12] Methods have been developed to transform or convert semiconducting SWCNTs to a specific conductivity type. These methods include chemical doping,[72,73,118,129] appropriate top dielectric selection on SWCNTs,[19,20,70,130,131] and appropriate metal contact selection.[132-136] With such methods, it is possible to convert unipolar FETs to ambipolar FETs and also ambipolar FETs to a single dominant conductivity type FETs.

*This chapter is based on Reference 125: Kim, B.; Geier, M. L.; Hersam, M. C.; Dodabalapur, A. Inkjet Printed Circuits on Flexible and Rigid Substrates Based on Ambipolar Carbon Nanotubes with High Operational Stability. *ACS Appl. Mater. Interfaces*, DOI: 10.1021/acsami.5b07727. B.K. and A.D. designed the experiments. B.K. carried out fabrication and characterization of devices. M.L.G. and M.C.H. provided semiconducting SWCNTs.

High performance SWCNT TFTs have been recently demonstrated by employing gravure and screen printing for deposition of electrodes and gate dielectrics;[56,137] however, SWCNTs from unwanted areas had to be removed/etched after blanket depositions of SWCNTs. This may be due to the fact that the rheology characteristics of typical SWCNT inks are not suitable for those printing techniques, where adequate ink viscosity is essential. Inkjet and aerosol jet printing are alternative deposition methods for printed SWCNT TFTs. A few groups have reported high performance SWCNT TFTs by using inkjet or aerosol jet printing for active SWCNTs deposition.[19,20,22,44,117,138,139] These two printing techniques allow patterning without the use of physical masks such as costly engraved metal masks. Printed patterns can be easily altered depending on the user's immediate demands since patterns are digitally designed. In addition, material consumption in both of these techniques is much lower compared to those of other printing techniques since the active materials are only utilized for additive patterning.

Herein, we present ambipolar SWCNT TFTs and their circuits, where most layers are deposited by inkjet printing, on flexible substrates as well as on rigid substrates. We have demonstrated various complementary circuits with inkjet printed SWCNTs (p-channel) and ZTO (n-channel), previously.[52,53,87,100] However, high annealing temperature for oxide layers prohibited implementing the complementary circuits on flexible substrates in that work. In this chapter, ambipolar SWCNT TFTs act as either n- or p-channel TFTs to enable complementary-like circuits to be implemented on flexible substrates. High performance SWCNT TFTs, where most layers are printed, have been reported;[56,117,137,140] however, integrated circuits based on those TFTs have not been reported yet. All layers, in this chapter, are patterned by inkjet printing without the use of rigid physical masks and photolithography. Bottom gate p-channel SWCNT TFTs are converted into ambipolar TFTs by a layer of Al_2O_3 deposited by ALD to create

complementary-like circuits. Inkjet printed Ag contacts inject both electrons and holes effectively, and lead to balanced hole and electron currents in ambipolar SWCNT TFTs. Integrated circuits based on these ambipolar TFTs are also demonstrated with high environmental and operational stability under ambient conditions.

6.2. EXPERIMENTAL

6.2.1. Device fabrication

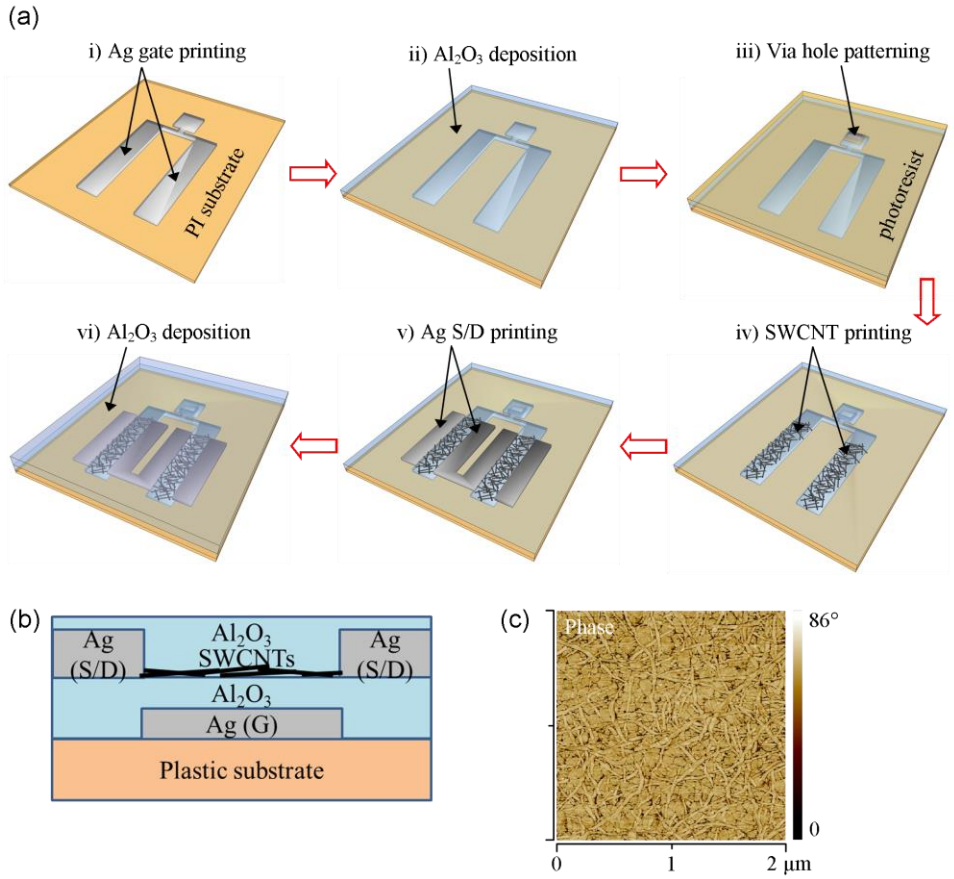

Figure 6.1: (a) Process flow for inkjet printed ambipolar SWCNT TFT-based inverters on a flexible substrate. (b) Schematic cross-section of an inkjet printed ambipolar SWCNT TFT on a PI substrate. (c) AFM image of SWCNTs in the channel region with a linear density of ~7 SWCNTs per µm.

Figure 6.1(a) illustrates the fabrication process of inkjet printed ambipolar SWCNT TFT-based inverters on a flexible PI substrate. Polyimide (DuPont™ Kapton® FPC polyimide film (125 μm thickness)) (PI) or glass substrates were cleaned by sequential sonication with acetone, methanol, and 2-propanol, followed by UV O_3 exposure for 5 min using a benchtop UV cleaner (PSD-UVT, Novascan). Commercial Ag nano-particle ink (SOLSYS EMD5603, Sun Chemical Corporation) was deposited by single pass of printing for bottom gate electrodes (~300 nm) on the substrates using a FUJIFILM Dimatix DMP-2800 printer with a 10 pL cartridge. The drop spacing was chosen to be 30 μm. After the gate printing, the substrates were placed on a hotplate at 200 °C for 30 min. An Al_2O_3 dielectric layer (43 nm) was deposited on the samples by ALD (Cambridge Nanotech) at 220 °C. After ALD, photoresist (AZ 5209-E) was spin coated on the Al_2O_3 layer. Via holes to the gate electrodes were patterned by five passes of acetone printing with a drop spacing of 40 μm on the photoresist coated samples and completed by wet etching with diluted buffered oxide etch (BOE) (H_2O:BOE = 40:1) for 2 min. After the remaining photoresist was removed by acetone, the surface of the dielectric was treated with UV O_3 for 10 min to promote wetting of inks.[22] SWCNTs (with >98% semiconducting SWCNTs prepared by DGU)[15,16] (average diameter: 1.4 nm, average length: ~1.4 μm)[36] were deposited on the treated surface of Al_2O_3 as ambipolar semiconductor layers by inkjet printing with a drop spacing of 40 μm. Further details on the preparation of the SWCNT ink is described in Chapter 2.2.1. After the printing of SWCNTs, the substrates were placed on a hotplate at 200 °C for 30 min to remove residual solvent. The Ag ink was inkjet printed twice for source/drain (S/D) electrodes (~500 nm) and interconnects with a drop spacing of 25 μm and the substrates were placed on a hotplate at 200 °C for 30 min. Finally, a second Al_2O_3 layer (43 nm) was deposited on the samples by ALD at 220 °C. The second Al_2O_3 layer converts p-type SWCNTs to

ambipolar SWCNTs, and also encapsulates the device to protect it. A schematic cross-section of the SWCNT TFT and the atomic force microscopy (AFM) image of SWCNTs are shown in Figure 6.1(b) and (c), respectively. Dimensional parameters of each layer in the TFTs are listed in Table 6.1.

Table 6.1: Thickness and dimension of each layer in the ambiplolar SWCNT TFTs with approximate W/L = 1400 μm/70 μm.

	Printed Ag gate	Al_2O_3 (dielectric/ encapsulation)	Printed SWCNTs	Printed Ag S/D
Thickness (nm)	~300	43	<10	~500
Approximate dimension (L (μm) × W (μm))	130 × 1500	Entire area	170 × 1500	150 × 1400

All of the processes, except for the Al_2O_3 deposition processes, were performed under ambient conditions in a cleanroom. The substrates were heated at 60 °C during the printing of Ag electrodes, but were unheated during the printing of SWCNTs and acetone. The TFTs were designed to possess channel length of 70 μm and width of 1400 μm, approximately. The PI substrates were taped on Si substrates using Kapton tape for easy handling during the process.

6.2.2. Electrical characterization of devices

The characteristics of TFTs and inverters were measured using a HP 4155C semiconductor parameter analyzer. The input signals for NAND and NOR gates were supplied using a Tektronix AWG 2005 arbitrary waveform generator. The output signals of NAND, NOR, and ROSCs were measured with a LeCroy WaveRunner 6030 oscilloscope. DC biases were supplied by the HP 4155C. All measurements were performed under ambient conditions.

6.3. RESULTS AND DISCUSSION

6.3.1. Type conversion of SWCNT thin-film transistors

Ag gate electrodes, via holes, SWCNTs, and Ag S/D electrodes were formed by inkjet printing sequentially. SWCNTs were patterned by direct additive printing, thus the active layers were not contaminated with photoresist residues and material consumption is significantly lower compared to previous printed SWCNT TFTs.[56,137] In addition, rinsing steps after SWCNT deposition were not required to remove additional surfactants or polymers,[19,20,44,56,117,137-140] which are used to prevent bundling of tubes or to sort semiconducting tubes, since they were not present in our SWCNT ink. This results in highly efficient material utilization.

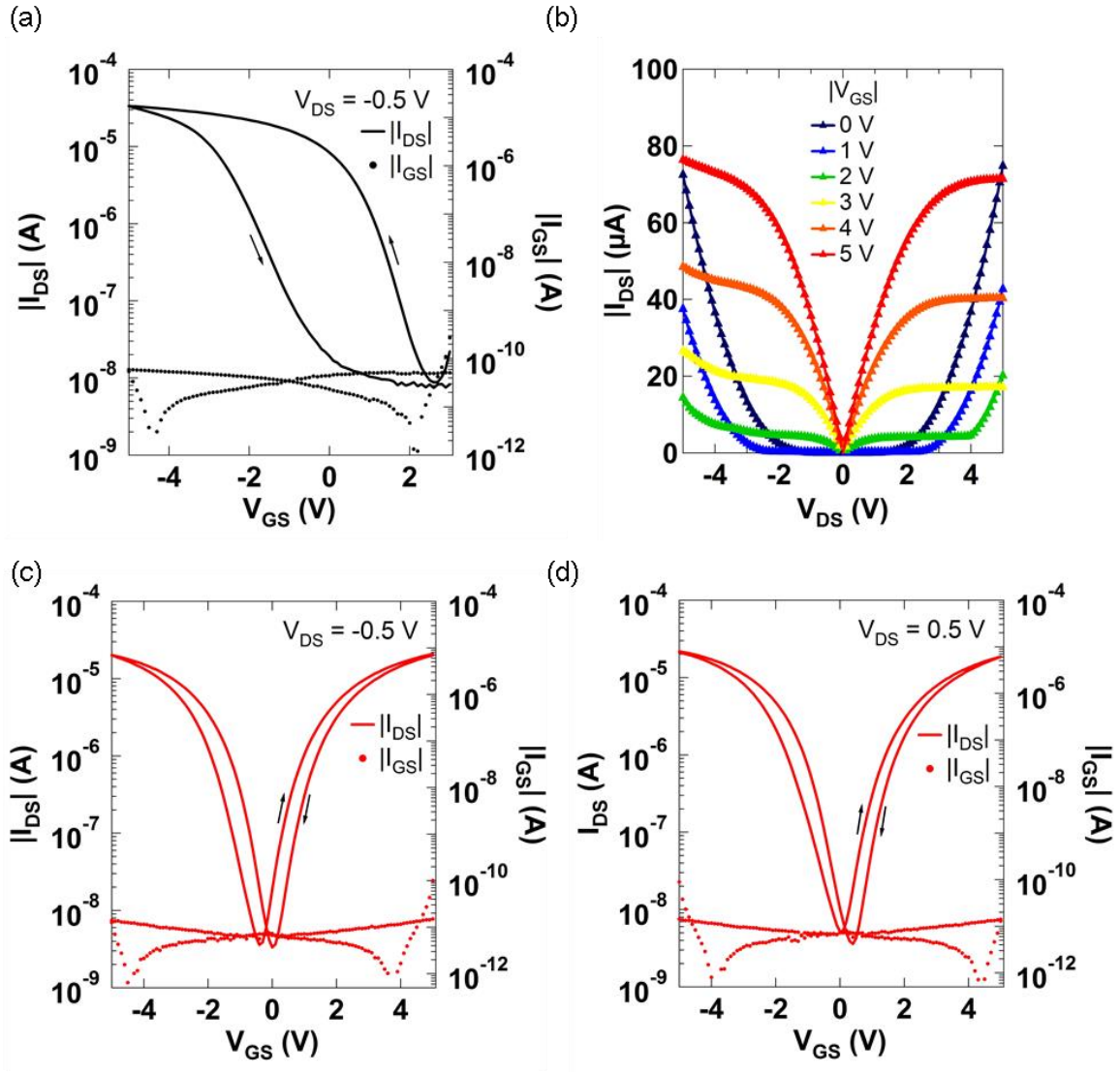

Figure 6.2: (a) Initial transfer characteristics of a typical bottom gate SWCNT TFT at $V_{DS} = -0.5$ V before Al_2O_3 deposition. (b) Output characteristics of the ambipolar SWCNT TFT after Al_2O_3 layer is deposited on top of the initial TFT. (c) Transfer characteristics of the ambipolar SWCNT TFT after Al_2O_3 layer is deposited on the initial TFT at $V_{DS} = -0.5$ V and (d) at $V_{DS} = 0.5$ V.

Inkjet printed bottom gate SWCNT TFTs on a PI film exhibit only p-channel operation with large hysteresis under ambient conditions before the deposition of an Al_2O_3 layer on top of the device, as shown in Figure 6.2(a). This is due to effects of

adsorbed O_2 and H_2O. The adsorbed molecules trap electrons and prohibit intrinsic ambipolar operation of SWCNT TFTs, and also cause hysteresis in SWCNT TFTs.[10, 12,141] The TFTs exhibit intrinsic field-effect mobility of 17.5 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} of 3.8×10^3 at $V_{DS} = -0.5$ V (Figure 6.2(a)) before deposition of the Al_2O_3. The mobility value was extracted by the following eq 6.1:

$$\mu = \frac{L}{W} \times \frac{1}{C_i} \times \frac{1}{V_{DS}} \times \frac{dI_{DS}}{dV_{GS}} \qquad \text{(eq 6.1)}$$

where $L = 70$ μm is the channel length, $W = 1400$ μm is the channel width, and C_i is the intrinsic capacitance for random network SWCNT TFTs. In the case of random network SWCNT TFTs with thin dielectrics, a more rigorous capacitance model should be considered instead of the parallel plate capacitance model in order to avoid an overestimation of the capacitance value.[36,51] The intrinsic capacitance, C_i, is defined in eq 6.2:

$$C_i = \{\frac{1}{2\pi\varepsilon_0\varepsilon_{Al_2O_3}} \ln[\frac{\Lambda_0}{R} \frac{\sinh(2\pi t_{Al_2O_3} / \Lambda_0)}{\pi}] + C_Q^{-1}\}^{-1} \Lambda_0^{-1} \qquad \text{(eq 6.2)}$$

where $\Lambda_0^{-1} = 7$ tubes/μm is the linear density of SWCNTs, ε_0 is the vacuum permittivity, $\varepsilon_{Al2O3} = 7.82$ is the dielectric constant of the Al_2O_3 layer, $t_{Al2O3} = 43$ nm is the thickness of the Al_2O_3 layer, $C_Q = 4.0\times10^{-10}$ F m^{-1} is the quantum capacitance of SWCNTs,[51] and $R =$ 0.7 nm is the average radius of SWCNTs.

The intrinsic ambipolarity of SWCNT is recovered after an Al_2O_3 layer is deposited by ALD on top of the fully fabricated device. The p-channel SWCNT TFTs (Figure 6.2(a)) convert into ambipolar TFTs as shown in Figure 6.2(b), (c), (d). This operational mode transformation is attributed to the combined effects of positive oxide charges in high-κ dielectrics and desorption of O_2 and H_2O during the ALD growth process.[70] Figure 6.2(b) shows output characteristics of the ambipolar SWCNT TFT, where electron and hole currents are very well balanced. The degree of balance in

electron and hole currents can be controlled by altering ALD process conditions and by the selection of different S/D contact materials and high-κ dielectrics.[70] This well-balanced ambipolar transport in ambipolar semiconductors[74,111,142,143] exhibit advantages, such as the use of only one active semiconductor and fewer process steps to fabricate complementary/complementary-like circuits, over n- or p-dominant ambipolar semiconductors.

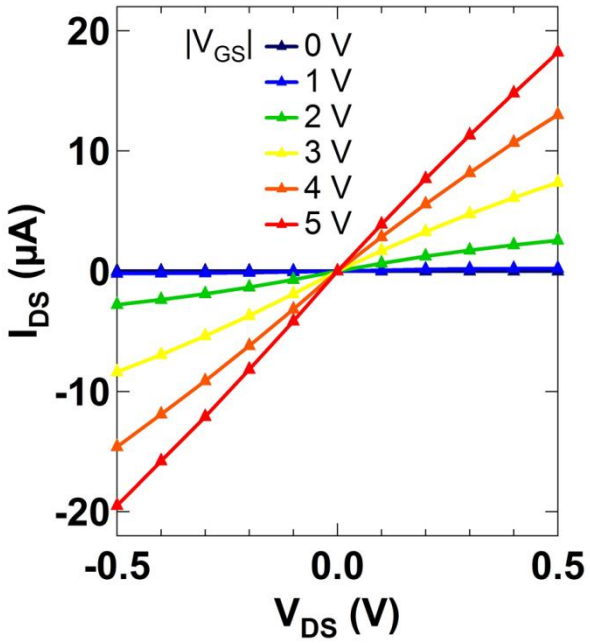

Figure 6.3: Output characteristics of the ambipolar SWCNT TFT in the linear regime.

Typical output characteristics of ambipolar TFTs, exhibiting typical minority carrier injection related current increases in addition to majority carrier current, can be seen. The output characteristics in the linear regime (Figure 6.3) indicate that the contact between SWCNTs and Ag electrodes are ohmic for the injection of both holes and electrons. This suggests that low-cost inkjet printed Ag electrodes are suitable contacts for ambipolar SWCNT TFTs in place of expensive vacuum deposited Au electrodes,

which have been hitherto employed as contacts in ambipolar TFTs.[19,20,52,62,74,111,120,138,139,142-145] Figure 6.2(c), (d) shows transfer characteristics of the ambipolar SWCNT TFT at V_{DS} = −0.5 V and 0.5 V, respectively (I_{DS}-V_{GS} on linear scale is shown in Figure 6.4). The hysteresis presented in the initial TFT (Figure 6.2(a)) is greatly reduced (from 3 V to 0.6 V) in the ambipolar TFT after the Al_2O_3 layer is deposited. The sum value of $|I_{on}|$ at V_{GS} = −5 V (20.1 µA in Figure 6.2(c)) and 5 V (18.6 µA in Figure 6.2(d)) in the ambipolar TFT is similar to the value of $|I_{on}|$ at V_{GS} = −5 V (33.4 µA in Figure 6.2(a)) in the initial p-channel TFT. Table 6.2 summarizes device characteristic parameters (mobility, log (I_{on}/I_{off}), threshold voltage (V_{th}), subthreshold swing (S.S.)) of ambipolar SWCNT TFTs in the linear regime at n- and p-channel accumulation-mode operation. Comparisons of other representative ambipolar semiconductors in the literature can be found in Table 5.1.

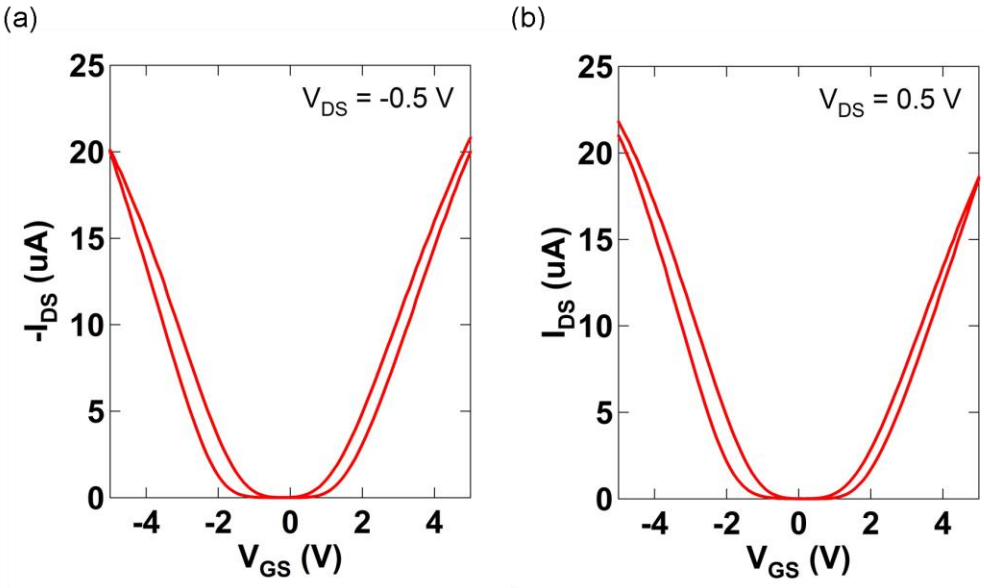

Figure 6.4: (a) Transfer characteristics (on linear scale) of the ambipolar SWCNT TFT after Al_2O_3 layer is deposited on the initial TFT at V_{DS} = −0.5 V and (b) at V_{DS} = 0.5 V.

Table 6.2: Device characteristic parameters of ambipolar SWCNT TFTs at n- and p-channel operation modes. The parameters were extracted from 8 different TFTs.

	mobility ($cm^2\ V^{-1}\ s^{-1}$)	$\log(I_{on}/I_{off})$	V_{th} (V)	S.S. (V/dec)
n-channel	12.5 ± 4.2	3.18 ± 0.37	1.82 ± 0.26	0.54 ± 0.14
p-channel	14.7 ± 5.0	3.43 ± 0.37	−1.31 ± 0.30	0.48 ± 0.08

6.3.2. Ambipolar SWCNT inverter

Various logic gates were fabricated based on the ambipolar SWCNT TFTs. The most basic building blocks of digital logic, inverters (NOT gates), were constructed on a PI film by connecting two ambipolar TFTs as shown in the inset of Figure 6.5(a). Two TFTs, which compose an ambipolar inverter, exhibit balanced electron and hole currents, thus they can operate as either pull-up or pull-down TFTs. Therefore, V_{DD} and *GND* terminals can be switched or the inverters can operate in the third quadrant of Figure 6.5(a) as well as in the first quadrant. Voltage transfer characteristics of the inverter were measured at different positive and negative values of V_{DD} (±3 V to ±7 V) and V_{IN} as shown in Figure 6.5(a). Typically, ambipolar inverters do not show complete rail-to-rail swing and their power consumption is higher than that of complementary inverters since one of the TFTs cannot be completely turned off.[52] Figure 6.5(b) shows DC gains ($|dV_{OUT}/dV_{IN}|$) of the inverter and maximum gains are larger than 15 when $|V_{DD}| = 7$ V.

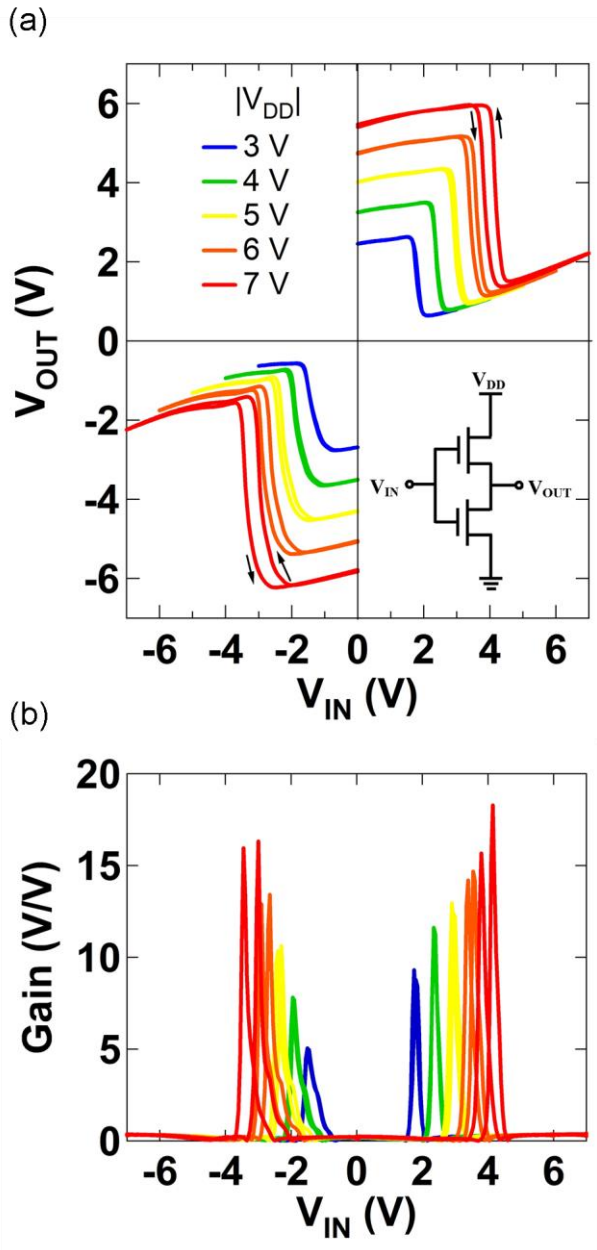

Figure 6.5: (a) Voltage transfer characteristics (VTCs) of the ambipolar SWCNT-based inverter when both V_{DD} and V_{IN} are positive and negative. Inset shows a circuit diagram of the ambipolar inverter. (b) DC gains ($|dV_{OUT}/dV_{IN}|$) of the ambipolar SWCNT-based inverter corresponding to its VTCs.

6.3.3. NAND/NOR gate based on ambipolar SWCNT transistors

NAND and NOR gates on a glass substrate are also demonstrated. Two different logic functions (NAND and NOR) can be performed in a single device when ambipolar TFTs are employed.[120,144,145] Four ambipolar SWCNT TFTs were connected as shown in Figure 6.6(a) to construct NAND or NOR logic gates. For a NAND logic operation, two TFTs connected in parallel work as p-TFTs and the other two TFTs connected in series work as n-TFTs. The output signals shown in Figure 6.6(b) only reach to LOW when both input signals are HIGH as a NAND gate. NOR logic functions are achieved by simply flipping DC biases (V_{DD} and *GND*) in the same device. For a NOR logic operation, two TFTs connected in series work as p-TFTs and the other two TFTs connected in parallel work as n-TFTs. The output signals shown in Figure 6.6(c) only reach to HIGH when both input signals are LOW as a NOR gate. Both NAND and NOR gates operate well at low operation voltages of 2 V with 100 Hz input signals.

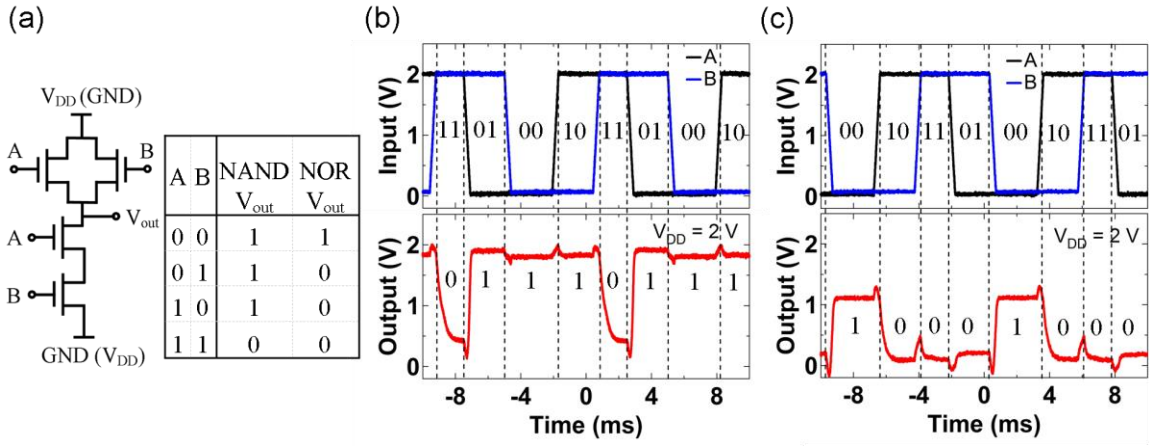

Figure 6.6: (a) Circuit diagram of an ambipolar SWCNT-based NAND (NOR) gate and its truth table. The bias conditions in parenthesis are for a NOR gate. (b) Dynamic response of a typical NAND logic gate on a glass substrate at V_{DD} = 2 V when 100 Hz input signals A and B are applied. (c) Dynamic response of a typical NOR logic gate on a glass substrate at V_{DD} = 2 V when 100 Hz input signals A and B are applied.

6.3.4. Ambipolar SWCNT ring oscillator

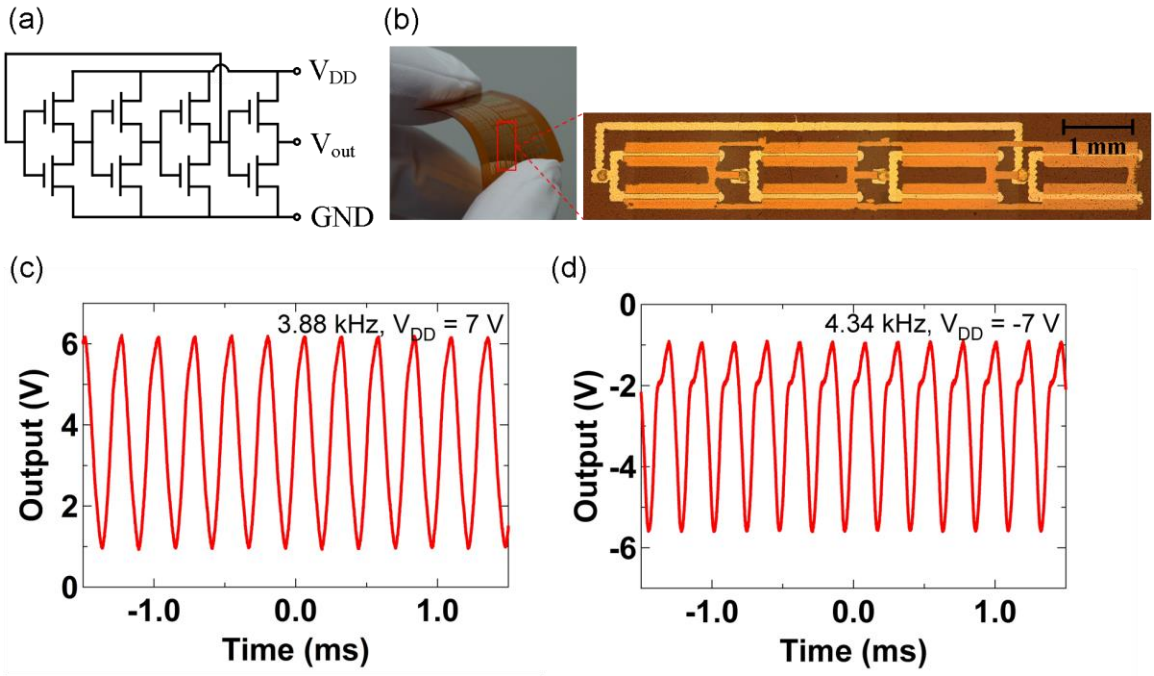

Figure 6.7: (a) Circuit diagram of an ambipolar SWCNT-based three-stage ROSC with a buffer stage. (b) Optical image of inkjet printed ambipolar SWCNT-based circuits on a flexible substrate and the micrograph of the three-stage ROSC. (c) Output signals of the ROSC at V_{DD} = 7 V and (d) at V_{DD} = −7 V.

Three-stage ROSCs were fabricated on a PI film to further demonstrate the potential of ambipolar SWCNT TFTs in integrated circuits. Three ambipolar SWCNT TFT-based inverters were connected in a loop with a buffer ambipolar inverter stage as shown in Figure 6.7(a). Figure 6.7(b) shows an optical image of the inkjet printed circuits on a flexible substrate and a micrograph of the three-stage ROSC. The overlap between gates and sources or drains in ROSCs is designed to be ~30 µm to ensure enough margins for alignments between the layers. Figure 6.7(c), (d) shows output signals of the ROSC at V_{DD} = 7 V and −7 V, respectively. The ROSC can operate at either positive or negative values of V_{DD} (±3 V to ±7 V) (Figure 6.8(a), (b)) since the constituent inverters are based on ambipolar SWCNT TFTs as described before. The propagation delay per stage, *t*, was

calculated using the equation $t = 1/(2Nf)$, where $N = 3$ is the number of stages and f is the oscillation frequency. The propagation delay per stage is 43 µs and 38 µs at V_{DD} = 7 V and −7 V, respectively (Figure 6.9).

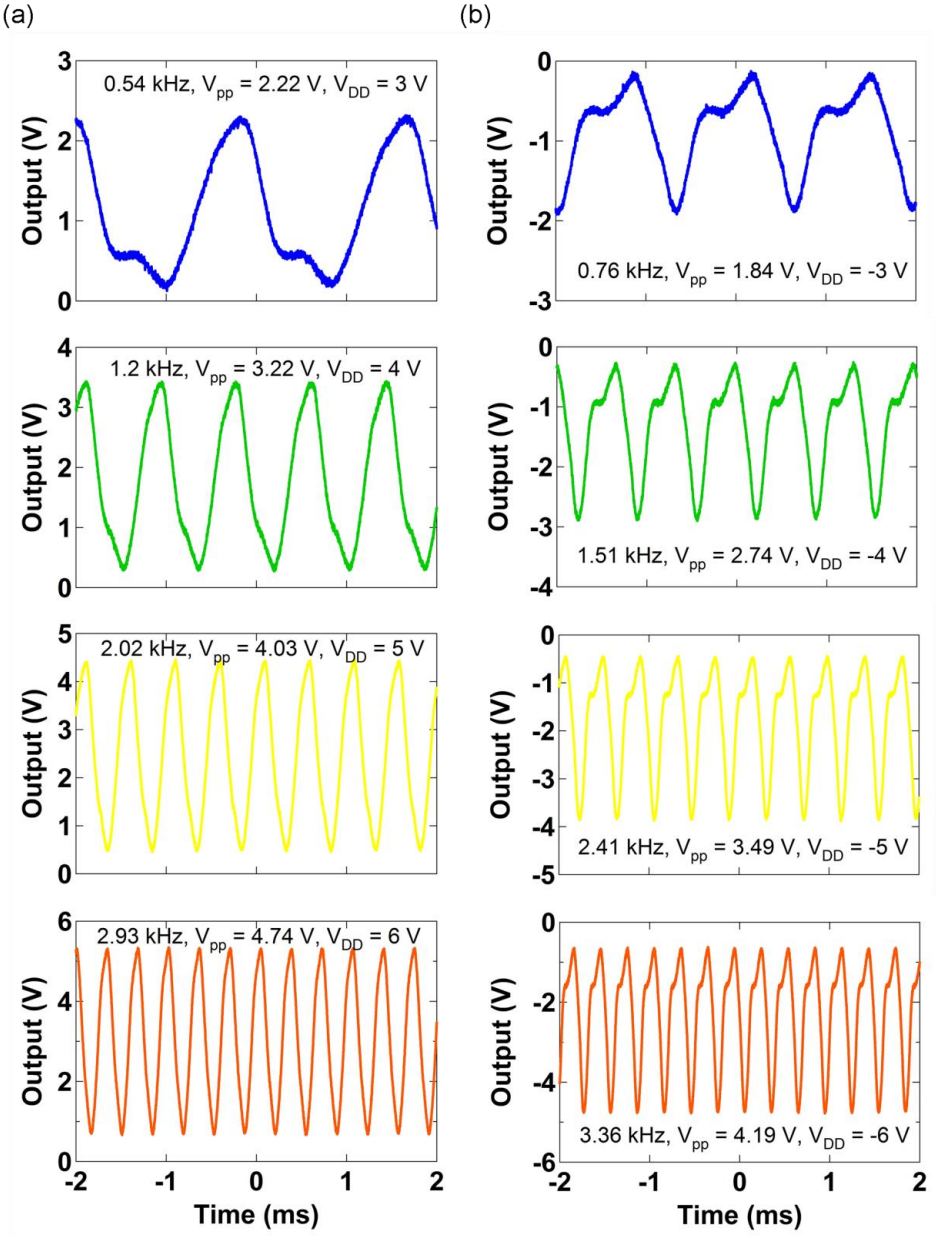

Figure 6.8: (a) Output signals of the three-stage ROSC at different positive values of V_{DD} and (b) at different negative values of V_{DD}.

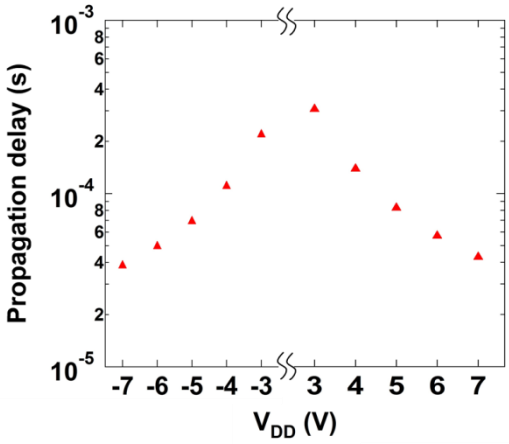

Figure 6.9: Propagation delay per stage of the three-stage ROSC as a function of V_{DD}.

The oscillation frequency of ROSCs is determined by different device parameters as described in eq 6.3:[106]

$$f \propto \frac{1}{NR_{on}C} \qquad \text{(eq 6.3)}$$

where N is the number of stages, R_{on} is the on-resistance which can be approximated as $R_{on} = 1/(\mu C_{ox}(W/L)(V_{GS} - V_{th}))$, and C is the output capacitance of each stage. In this work, f is mainly limited by large L and large gate overlap, which substantially increases C. If a better device design with shorter L, smaller gate overlap (parasitic capacitance) and C, and higher μ by material engineering is employed, f can be further improved.[52]

Environmental and operational stability of circuits under ambient conditions is one of the main challenges in printed electronics for commercial applications. Numerous TFT-based (either printed or non-printed) ROSCs have been demonstrated, however, there have been only a few studies that report their operational stability.[19,52,146] The three-stage ROSC on a flexible substrate was continuously operated for 83 h under ambient conditions at V_{DD} = 3 V in order to demonstrate environmental and operational stability of the ambipolar SWCNT-based circuits. The oscillation frequency increases up to ~600

Hz (from 536 Hz at t = 0, increase of 11.9 %), then stabilizes and eventually slightly decreases (Figure 6.10(a)), while the peak-to-peak voltage (V_{pp}) remains almost the same (Figure 6.10(b)). The decrease in the frequency, from the stabilized frequency (600 Hz) to the frequency measured (549 Hz) after 83 h of operation, is 8.5 %. Figure 6.11 shows the output characteristics of the ROSC at specific time points.

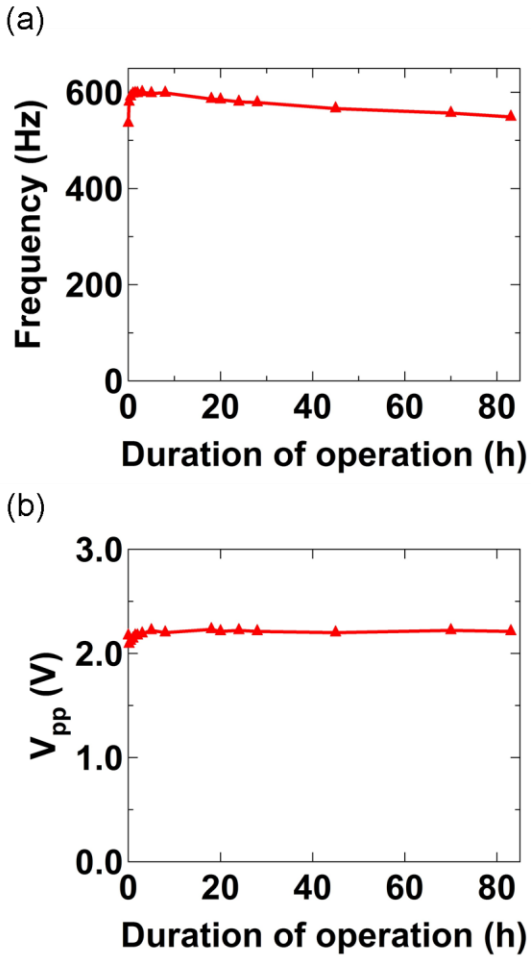

Figure 6.10: Characteristics of the ROSC operated continuously at V_{DD} = 3 V under ambient conditions. (a) Oscillation frequency as a function of duration of operation. (b) V_{pp} of output waveforms as a function of duration of operation.

During the measurement, each of stages switched on and off more than 150 million times. Considering that the performance degradation is less than 10% after 83 h of continuous operation under ambient conditions, the operating lifetime of the SWCNT circuits are expected to be considerably long. The Al_2O_3 layer employed in this chapter not only converts p-type SWCNT TFTs into ambipolar TFTs, but also passivates devices effectively.[70,147] The ALD Al_2O_3 layer on top of the devices results in significantly higher stability compared to that of electrolyte gated transistor-based printed circuits,[19,146] which have only been measured under vacuum or inert conditions, as well as other printed circuits.[52]

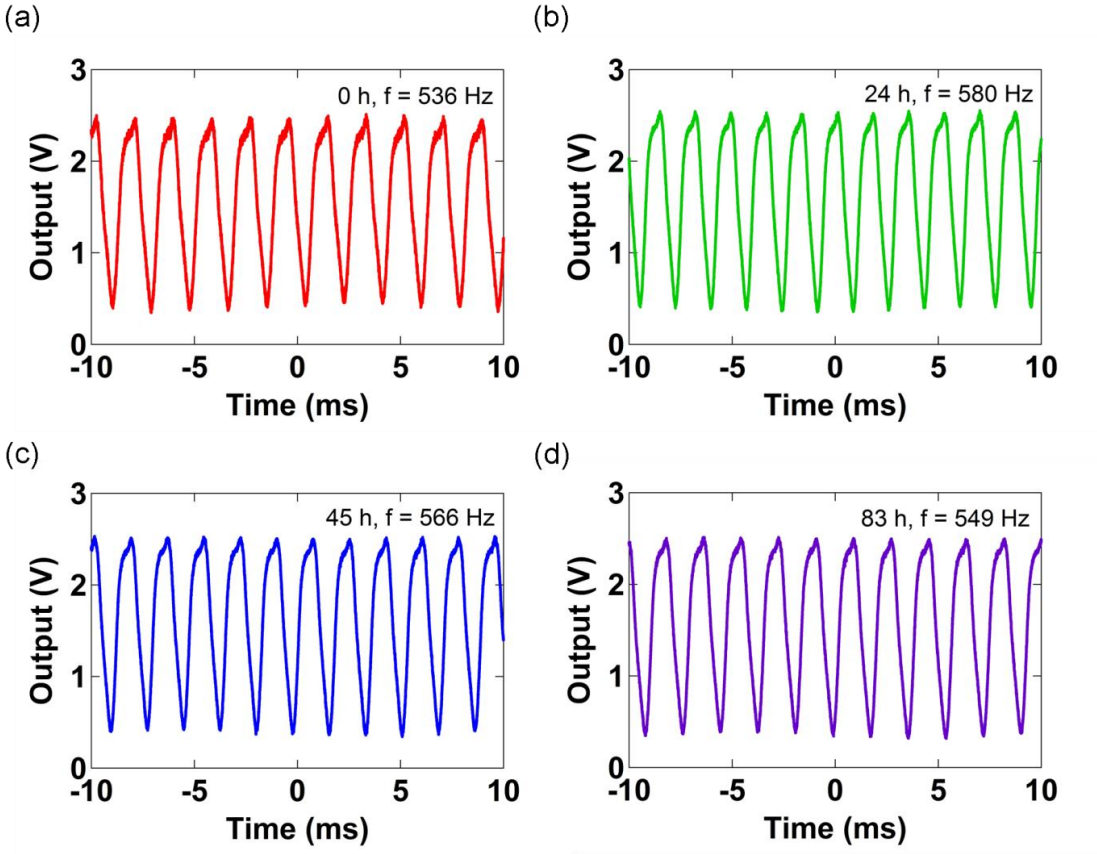

Figure 6.11: Output signals of the three-stage ROSC operated continuously under ambient conditions at V_{DS} = 3V for (a) 0 h, (b) 24 h, (c) 45 h, and (d) 83 h.

6.4. CONCLUSION

Ambipolar SWCNT TFT-based circuits using inkjet printing have been demonstrated on flexible and rigid substrates with high stability. All patterns have been formed by inkjet printing without the use of rigid physical masks and photolithography. In particular, cost-effective inkjet printed Ag has been employed as S/D electrodes in ambipolar TFTs, and it has shown that both holes and electrons can be injected effectively in place of Au electrodes, which are the most common S/D electrodes for ambipolar TFTs. NOT, NAND, NOR logic gates and three-stage ROSCs have been demonstrated with distinct features of ambipolar circuits. An ALD Al_2O_3 layer on top of devices transforms p-type SWCNTs into ambipolar SWCNTs, reduces hysteresis in TFTs, and results in high environmental and operational stability in circuit performance. This work demonstrates the great potential of random network SWCNTs as active semiconductors in low-cost, flexible and printed electronics.

Chapter 7. Conclusion

In this dissertation, various TFTs and circuits were demonstrated by using inkjet printed semiconductors. Amorphous zinc tin oxide and random network of single-walled carbon nanotubes were employed as n-channel and p-channel/ambipolar semiconductors, respectively, and these active semiconductors have showed great promise in printed thin-film electronics. Various supporting substrates (silicon wafer, glass, polyimide), dielectric layers (solution processed ZrO_2, ALD deposited Al_2O_3, bilayer of P(VDF-TrFE)/Al_2O_3), S/D contacts (Ti/Au, inkjet printed Ag), gate electrodes (global Si substrate, Pt, Ni, inkjet printed Ag) were employed in various circuit applications.

High performance (intrinsic mobility >30 $cm^2\ V^{-1}\ s^{-1}$, I_{on}/I_{off} >10^5) random network SWCNT TFTs were demonstrated by *single-pass* inkjet printing of SWCNTs. Modification of the bottom gate dielectric's surface energy by UV O_3 surface treatment enabled the formation of uniform and dense network of SWCNTs in the channel region with just *single-pass* inkjet printing. Complementary circuits including inverters, ROSCs, and D flip-flops were demonstrated based on inkjet printed SWCNTs (p-channel) and ZTO (n-channel) with high performance and good air-stability. The oscillation frequency of the complementary ROSC reached over 700 kHz, which is the fastest frequency for any reported ROSCs with printed semiconductors to date. It was also shown that the oscillation frequencies of these ROSCs can be linearly controlled by applied top-gate bias when additional gate dielectric and gate electrode are added on these ROSCs. In addition, threshold voltages in individual TFTs and switching thresholds in inverters can be also controlled systemically by top-gate bias.

Besides complementary circuits, complementary-like circuits were also demonstrated by employing a bilayer SWCNT/ZTO heterostructure or ambipolar SWCNTs. When SWCNTs are inkjet printed on top of inkjet printed ZTO layer, both electron and hole transport occurs mainly in ZTO and SWCNT layers, respectively, in a single TFT. ROSCs based on these bilayer ambipolar semiconductors showed the highest oscillation frequency among best reported ambipolar TFT-based ROSCs. Furthermore, ambipolar SWCNT TFTs and circuits were realized on flexible PI substrates with inkjet printed electrodes. An Al_2O_3 encapsulation layer which was deposited by ALD on top of bottom gate SWCNT TFTs not only converted p-channel TFTs to ambipolar TFTs, but also resulted in significantly higher operational and environmental stability.

For future work, all-inkjet printed circuits on flexible substrates can be realized by employing reliable and inkjet printable polymer dielectrics. If oxide semiconductors which can be formed at relatively low temperature are employed as n-channel semiconductors instead of ZTO formed at high annealing temperature in this dissertation, high performance complementary circuits can be implemented on flexible substrates as well. These complementary circuits along with ambipolar TFTs will enable a new class of circuits.

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